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Structural Optimization Study on Hybrid TFET with MoS_2 Channel and N+/P+ Si Tunnel Junction

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Abstract

This paper presents the structural optimization of hybrid TFET with MoS_2 as a channel and N+/P+ Si junction at the source edge on SOI substrate to improve the scalability of logic transistors for sub-0.5V application based on simulation works. It has been observed that the structural parameters such as channel thickness, gate oxide thickness, and gate-to-source overlap and halo width have significant effects on hybrid TFET characteristics in terms of threshold voltage, subthreshold slope, off-state leakage current and DIBL. The structural optimization to be obtained for further gate length scaling beyond 10nm is channel thickness (MoS_2) reduction to 1nm, gate-to-source underlap of -1nm, halo width of 1nm and gate oxide thickness of 0.8nm.

Keywords: MoS_2 FET, Band-to-band tunneling (BTBT), Low voltage operation, Field-effect transistor (FET), Tunnel FET (TFET), Silicon-on-insulator (SOI), Subthreshold slop, 2D channel FET, Heterogeneous structure.

INTRODUCTION

In recent logic technology nodes, much effort has been made to scale down gate length of MOSFET (Metal-Oxide-Semiconductor Field-Effect-Transistor) without remarkable short channel effect (SCE) for enjoying density and performance benefits. Bulk planar MOSFET is replaced by bulk FinFET structure to suppress the off-state leakage current [1], [2]. As gate pitch is decreased to 45nm and smaller, since gate length should be scaled down even to 10nm or less to guarantee the reasonable contact-hole dimension, alternative device structures such as nanowire and 2D channel FET attract much attention [3].

Since even bulk FinFETs have fundamentally the lowest subthreshold slope (SS) limit of 60mV/decade [4], several devices such as tunnel FETs (TFET), impact-ionization MOSFETs and NEMFET, etc. have been under intensive study to achieve extremely low standby leakage and low threshold voltage (Vth) for sub-0.5V supply voltage applications [4], [5]. Also, the hybrid FET device structure is proposed by applying 2D material such as MoS_2 as a channel and N+/P+ tunneling junction at the source edge to extend the scaling limit of TFETs by the increased intra-band tunneling with gate length less than 16nm, [6]. With this hybrid TFET, gate controllability is improved by 2D channel and the steep SS is achieved by N+/P+ tunneling junction at the source edge.

In this paper, the effect of structural parameters such as gate oxide thickness, channel thickness, gate-to-source overlap and halo width on the scalability of hybrid TFETs has been extensively investigated in terms of threshold voltage (Vth), SS, DIBL (drain-induced barrier lowering) and off-state leakage current (Ioff). The optimized hybrid TFET structure for scaling down gate length of logic transistors less than 10nm will be given based on systematic simulation results.

SIMULATIONS

Figure 1 shows the schematic structure of hybrid n-type TFET (NTFET) used in this study, where it has a single-gated p-i (MoS_2)-n structure and dopant pocket region (H, halo region) near the source region on SOI substrate to improve gate contribution on tunneling efficiency. Key parameters to be investigated for structural optimization of hybrid NTFET include channel and gate oxide thickness, halo width, and gate-to-source overlap.

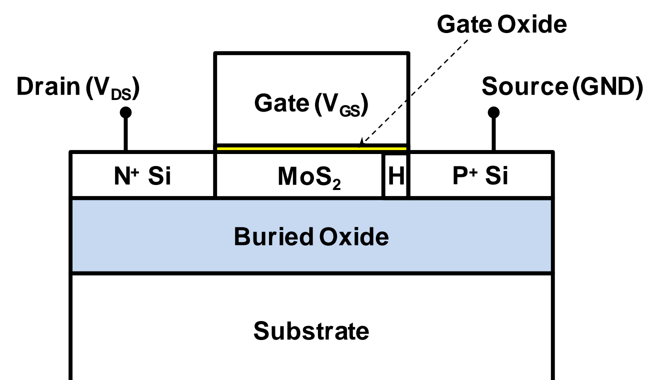

Figure 1. The schematic structure of hybrid n-type TFET (NTFET) used in this study, where it has a single-gated p-i (MoS_2)-n structure and dopant pocket region (H, halo region) near the source region on SOI substrate to improve gate contribution on tunneling efficiency.

The simulation tool to investigate the structural optimization of hybrid NTFET in this paper is SILVACO TCAD ATLAS [7]. BTBT (Band-to-Band Tunneling) mechanism has been modeled using the dynamic nonlocal path tunneling approach, taking into accounts the nonlocal generation of electrons and holes caused by direct and phono-assisted processes. The device parameters throughout this work (if not differently specified) are as the following: doping concentration of source (P+), drain (N+) and halo (N+) regions $N_D = N_A = 1 \times 10^{21}$ cm^{-3}; intrinsic channel (i-channel) doping concentration $N_D = 1 \times 10^{13}$ cm^{-3}; lifetime in the channel t = 1x 10^{-6} sec; gate work function eWF = 4.25 eV; supply voltage $V_{GS} = V_{DS} = 0.5$ V. Especially, MoS_2 channel is assumed to have physical properties such as bandgap of 1.4 eV @300K, permittivity of 4.0, and low field mobility of 60 $cm^2/V \cdot s$.

RESULTS and DISCUSSION

The structural optimization of hybrid NTFET has been carried out based on targeting its key electrical characteristics such as Vth, SS, DIBL, and Ioff, where typical targets are as following; one fourth of supply voltage for Vth, less than 60mV/dec for SS, less than 50mV for DIBL, and minimum for Ioff. Vth is defined as the gate voltage at which the drain current is 10nA/um.

Figure 2 (a) to (d) show the trend of electrical characteristics of hybrid NTFETs as a function of channel (MoS_2) thickness for different gate lengths of 4nm to 10nm, where they have halo width of 2nm, gate oxide thickness of 0.8nm, and gate-to-source overlap of 0nm. It can be seen from Fig. 2(a) to (d) that hybrid NTFET with gate length of 4nm shows typical device behavior only for extremely thin channel length of 1nm, even though they are seriously poor. Also, it has been observed that except for Vth case, the effect of channel thickness reduction become more significant for smaller gate length. The most significant improvement of channel thickness reduction is observed for DIBL behavior. This is believed to be due to the improvement of gate controllability with channel thickness reduction.

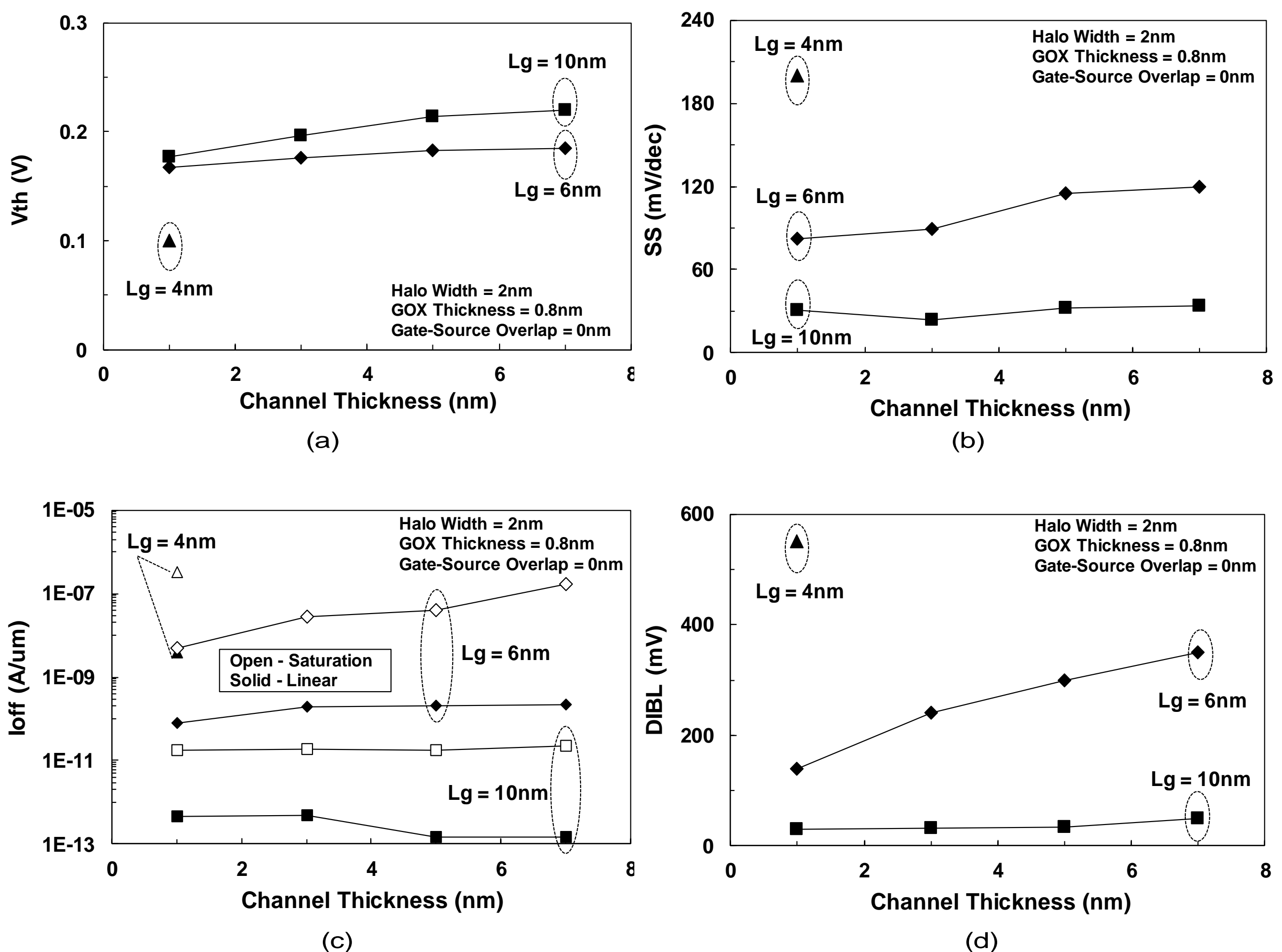

Figure 2. The trend of electrical characteristics of hybrid NTFETs as a function of channel (MoS_2) thickness for different gate lengths of 4nm to 10nm; Vth (a), SS (b), Ioff (c), and DIBL (d), where they have halo width of 2nm, gate oxide thickness of 0.8nm, and gate-to-source overlap of 0nm.

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Figure 3(a) and (d) shows the behaviors of electrical characteristics of hybrid NTFETs as a function of gate oxide thickness for different gate lengths of 4nm to 10nm, where they have channel (MoS_2) thickness of 3nm, halo width of 2nm, and gate-to-source overlap of 0nm. It has been observed from Fig. 3(a) that Vth shows two different trends with gate oxide thickness for gate lengths of 6nm and 10nm, and that hybrid NTFET with gate length of 4nm has negative Vth resulted from source-to-drain punch through current. Except for Vth, other electrical parameters such as SS, Ioff, and DIBL show relatively small dependency on gate oxide thickness. The reason is believed to be the fact that the channel potential is already controlled well due to reduced channel thickness of 3nm before applying gate oxide thickness scaling. That is, channel thickness scaling is more effective than gate oxide thickness reduction.

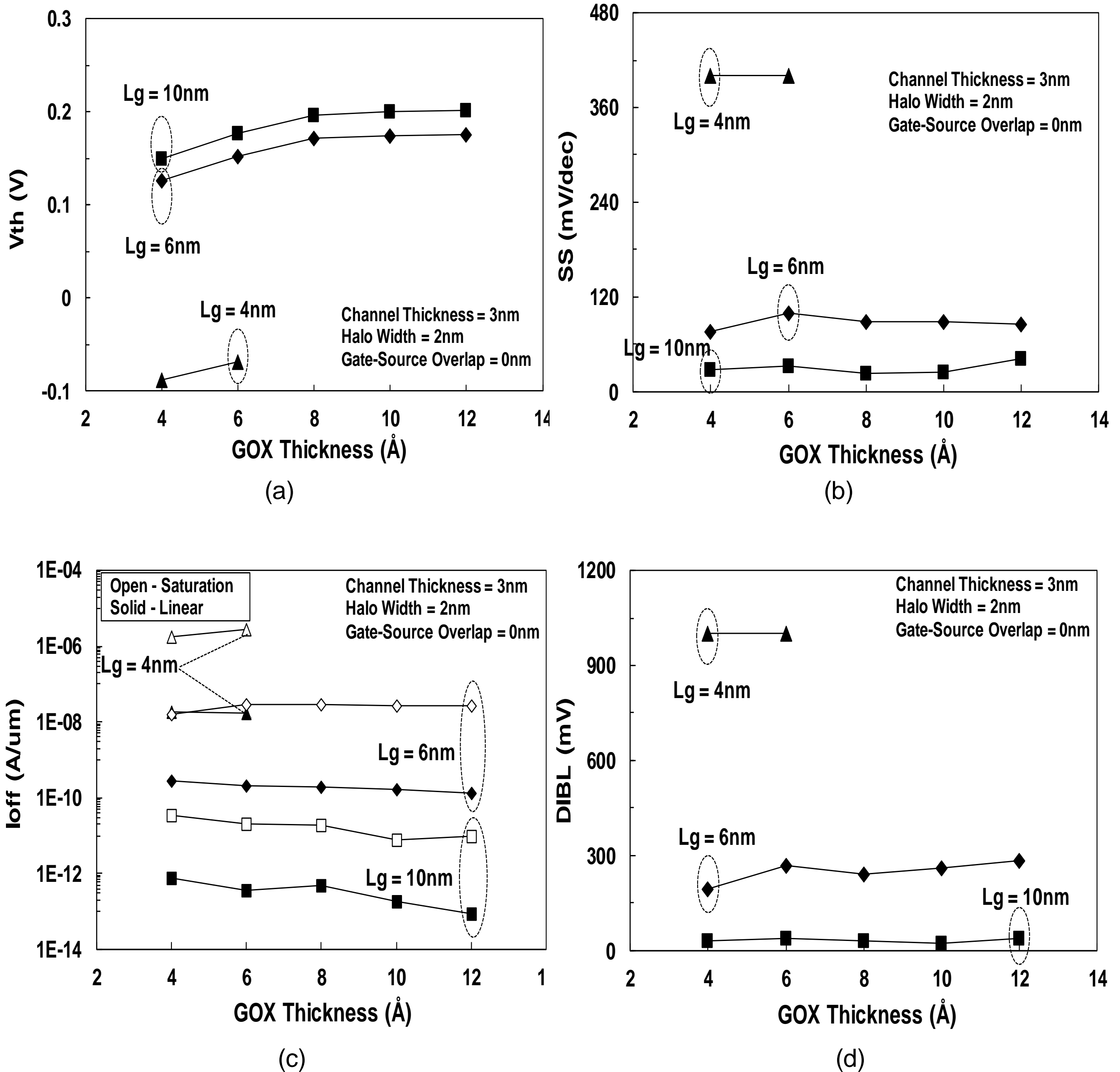

Figure 3. (a) and (d) shows the behaviors of electrical characteristics of hybrid NTFETs as a function of gate oxide thickness for different gate lengths of 4nm to 10nm; Vth (a), SS (b), Ioff (c), and DIBL (d), where they have channel (MoS_2) thickness of 3nm, halo width of 2nm, and gate-to-source overlap of 0nm.

The trend of electrical characteristics of hybrid NTFETs with gate length of 10nm as a function of width of halo region (i.e., N+ pocket region at the source edge) is shown in Fig. 4 (a) to (d), where they have channel (MoS_2) thickness of 3nm, gate oxide thickness of 0.8nm, and gate-to-source overlap of 0nm. It has been observed that Ioff shows significant behavior with halo width, but that other parameters such as Vth, SS, and DIBL have very little dependency on halo width. Since hybrid NTFETs have highly doped N+ region (halo) at the source (P+) edge to improve the carrier injection into the channel, the tunneling current at the abrupt junction is already expected. However, as shown in Fig. 4(c), since Ioff is increased very slightly with halo width of 1nm, the device performance can be optimized by applying the minimized halo region.

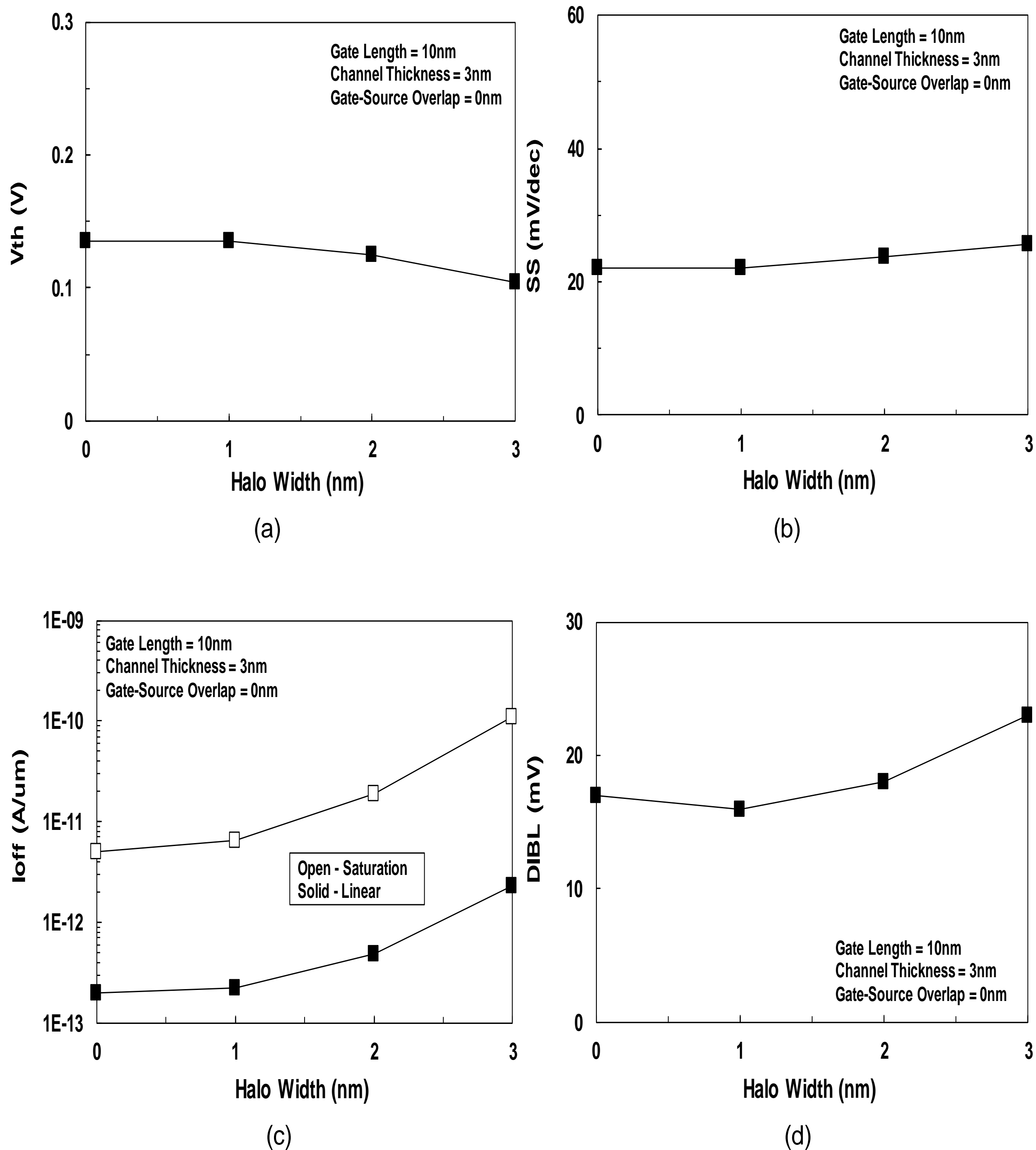

Figure 4. The trend of electrical characteristics of hybrid NTFETs with gate length of 10nm as a function of width of halo region (i.e., N+ pocket region at the source edge); Vth (a), SS (b), Ioff (c), and DIBL (d), where they have channel (MoS_2) thickness of 3nm, gate oxide thickness of 0.8nm, and gate-to-source overlap of 0nm.

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Figure 5(a) and (d) shows the behaviors of electrical characteristics of hybrid NTFETs as a function of gate-to-source overlap for different gate lengths of 4nm to 10nm, where they have channel (MoS_2) thickness of 3nm, gate oxide thickness of 0.8nm, and halo width of 2nm. As shown in Fig. 5(a), Vth shows the minimal point at gate-to-source overlap of 0nm (i.e., just-lap), but both gate-to-source underlap (i.e., negative value) and overlap (i.e., positive value) increase Vth. Even though gate-to-source overlap increase Vth, the aggressive scaling of gate length causes the source-to-drain punch due to increased intra-band tunneling. However, this source-to-drain punch phenomena with scaled gate length may be released by applying the gat-to-source underlap structure, as shown in Fig. 5(a). It has been observed from Fig. 5(b) that SS is much degraded for scaled gate length by applying gate-to-source overlap structure, and that the gate-to-source underlap structure gives SS less than 60mV/dec even for gate length of 6nm. The effectiveness of gate-to-source underlap structure on Ioff seems to be straightforward, as shown in Fig. 5(c), showing that Ioff decreases exponentially from overlap (2nm) to underlap (-2nm). Also, gate-to-source underlap structure helps improving DIBL behavior with gate length aggressively scaled blew 10nm, as shown in Fig. 5(d), However, hybrid NTFET with gate length of 4nm shows very degraded short channel effect even with gate-to-source underlap of -2nm.

Based on the trend between structural parameters and electrical characteristics from Fig. 2 to Fig. 5., the optimized structure of hybrid NTFET can be proposed. Figure 6 shows the optimized structure of hybrid NTFET for scaling gate length less than 10nm, where it has channel thickness of 1nm, gate oxide thickness of 0.8nm, halo width of 1nm, and gate-to-source overlap of -1nm (i.e., 1nm underlap)

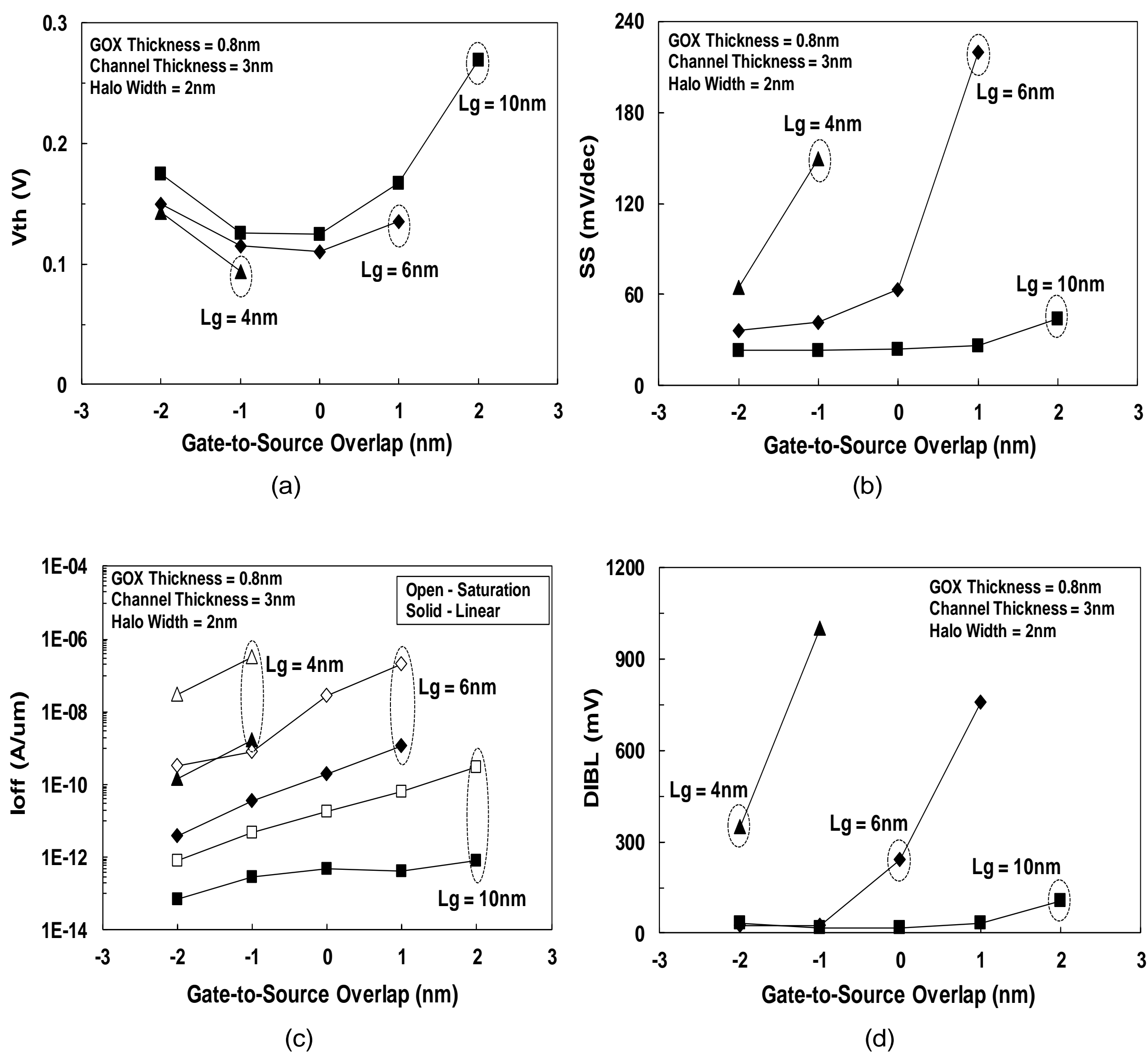

Figure 5. Threshold voltage and off-state leakage current behaviors of the proposed hybrid FET with gate length scaling for different MoS_2 thickness; Vth (a), SS (b), Ioff (c), and DIBL (d), where all simulated devices have gate oxide thickness of 0.8nm, halo width of 2nm, and gate-to-source overlap of 0nm.

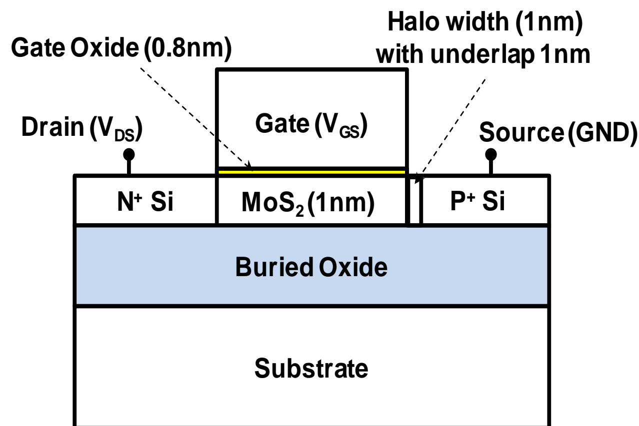

Figure 6. The optimized structure of hybrid NTFET for scaling gate length less than 10nm, where it has channel thickness of 1nm, gate oxide thickness of 0.8nm, halo width of 1nm, and gate-to-source overlap of -1nm (i.e., 1nm underlap)

CONCLUSIONS

In this paper, the structure of hybrid NTFET has been optimized in terms of scalability by correlating structure parameters and electrical characteristics. Among structural parameters, channel thickness and gate-to-source overlap are key design parameters for scaled devices. It is obtained that the optimum structure of hybrid NTFET with gate length of 6nm has channel thickness of 1nm, gate oxide thickness of 0.8nm, halo width of 1nm, and gate-to-source overlap of -1nm (i.e., 1nm underlap). It is believed that the structure of hybrid PTFET can be optimized by the same method in this paper.

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