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Hybrid Symmetrical Cascaded Multilevel Inverter having reduced number of Switches and DC Sources

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Abstract

Research in several new topologies of Multilevel inverter(MLI) has been carried out rapidly day by day. Recently several topologies have been introduced achieving higher levels with reduced device couns and DC sources .In this paper a new hybrid symmetric MLI is proposed .This topology has reduced number of controlled switches, Dc sources and numbers of capacitors which are very less compared to all the conventional topologies existed before. It reduces cost,size,complexity and hence enhances inverter efficiency.

Keywords: Symmetric MLI, Asymmetric MLI ,Hybrid topology, THD, Modulation Index(MI)

INTRODUCTION

As the MLI has less THD and less switching losses it receives demanding popularity in terms of topology and in control scheme in the field of medium voltage, high power Dc/Ac conversion system[1].The traditional MLIs are of various types and many of the literature are published with respect to their advantages and disadvantages [2].Among all the existing topologies cascaded Multilevel inverter(CMLI)is popular because of its simplicity but it requires a number of isolated Dc sources[3].On the basis of the Dc source voltages the CMLI are of two types i.e Symmetrical MLI and Asymmetrical MLI[4].From last few years different topologies have been developed by utilizing unidirectional and bidirectional switches [5]-[7].Though by the implementation of asymmetrical MLI the number of levels increases giving reduced THD ,asymmetric converter is not really appreciated because they are not suitable for high voltage industrial application for its variable DC sources.[8]-[9].However the proposed topology can be hybridized further to achieve higher levels[10]- [11].

RESEARCH METHOD

A. Existing Topology

It has two voltage sources V_1 and V_2 along with two capacitors C_1 and C_2 which act like voltage divider circuit[6]. If the values of $V_1 = V_2$ it is treated as symmetrical otherwise asymmetrical. Existing Topology produces 7/9/11 levels with certain voltage combinations[10].

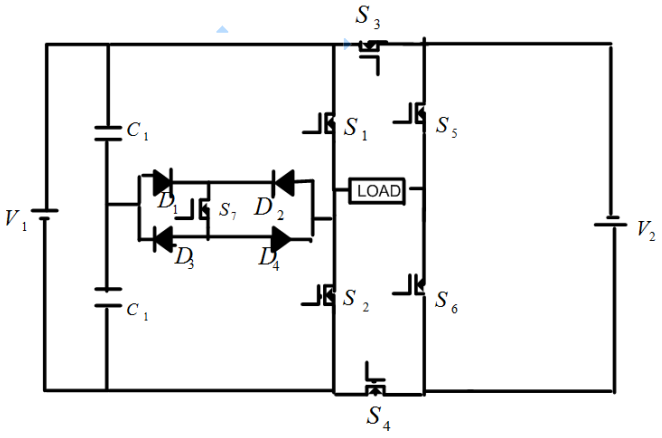


Figure 1: Existing Topology

For 7 level asymmetrical $V_1=2V$, $V_2=V$ and $V_{dc}=V$.
For 9 level symmetrical $V_1=V_2=V$.For 11 level asymmetrical $V_1=4V$, $V_2=V$ in this existing topology .

B. Modified Topology

Existing Topology produces upto 11 levels and higher levels have not been achieved with this topology .Hence to achieve higher levels (i.e 13^{th} and 17^{th}) modified Topology has been proposed. With increase in number of levels THD had been reduced significantly in asymmetrical configuration .However his modified topology also achieve 9levels in symmetrical configuration.

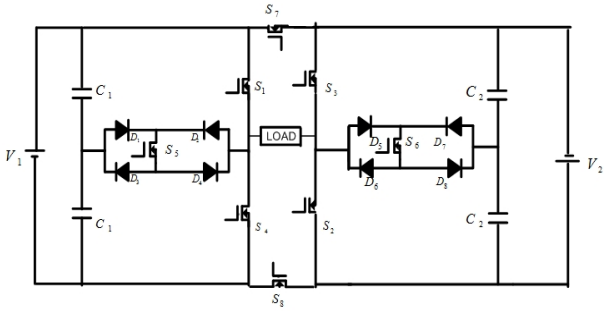


Figure 2: Modified Topology

Table 1: Switching States

1 3 Levels				17 Levels		
Output	Conducting switches	Conducting Diodes		Output	Conducting switches	Conducting Diodes
Vdc	S5 , S2 , S8	D1,D4		Vdc	S5 , S2 , S8	D1,D4
2Vdc	S6 , S4 , S8	D5,D6		2Vdc	S1 , S2 , S8	NIL
3Vdc	S5 , S6 , S8	D1,D4,D5,D8		3Vdc	S8 , S4 , S6	D5,D8
4Vdc	S8 , S4 , S3	NIL		4Vdc	S8 , S5 , S6	D1,D2,D3,D4
5Vdc	S8 , S5 , S3	D1,D4		5Vdc	S1 , S6 , S8	D5,D8
6Vdc	S8 , S1 , S3	NIL		6Vdc	S8 , S4 , S3	NIL
0	S1 , S3 , S7	NIL		7Vdc	S8 , S5 , S3	D1,D4
-Vdc	S5 , S3 , S7	D2,D3		8Vdc	S8 , S1 , S3	NIL
-2Vdc	S7 , S1 , S6	D7,D6		0	S1 , S2 , S3	NIL
-3Vdc	S5 , S6 , S7	D7,D6,D2,D3		- Vdc	S7 , S3 , S5	D2,D3
-4Vdc	S2 , S1 , S7	NIL		-2Vdc	S7 , S3 , S4	NIL
-5Vdc	S2 , S5 , S7	D2,D3		-3Vdc	S6 , S1 , S7	D7,D6
-6Vdc	S2 , S4 , S7	NIL		-4Vdc	S6 , S5 , S7	D2,D3,D7,D6
x	x	x		-5Vdc	S7 , S6 , S4	D7,D6
x	x	x		-6Vdc	S2 , S1 , S7	NIL
x	x	x		-7Vdc	S2 , S7 , S5	D2,D3
x	x	x		-8Vdc	S2 , S4 , S7	NIL

The modified topology produces as mentioned in table 1. This section of the paper represents various switching states of proposed asymmetrical cascaded MLI. It shows V_1=V/2, V_2=V where V $_{dc}$ =V/4 to generate 13 levels and V_1=V, V_2=3V where V $_{dc}$ =V/2, to generate 17 levels. **T**his section also explains binary configuration where one source voltage value is double the value of other and trinary where one source voltage value is thrice the value of other source voltage.

C. Hybrid Topology

Two or more basic units can be added as shown in fig.3 to achieve higher levels.The switching states of the topology has been represented in Table 2.It represents the symmetrical configuration where all the source voltages are same in magnitude.V1=V2=V and Vdc=V/2.In his case all he voltage sources are equal in magnitude giving symmetrical configuration of cascaded multilevel inverter.

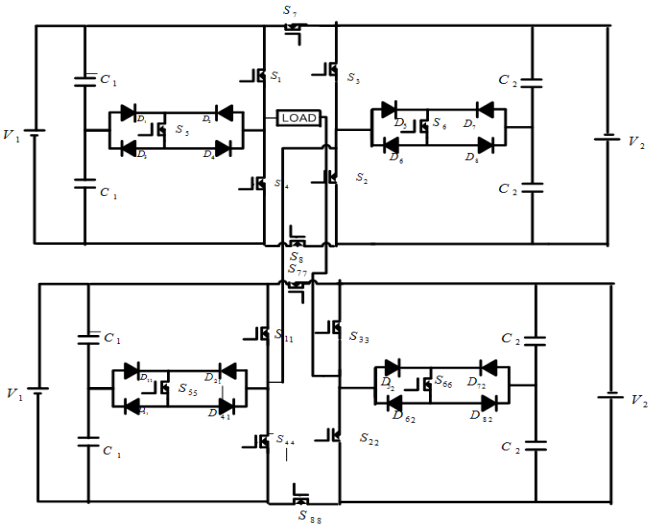


Figure 3: Hybrid Topology

Table 2: Switching States

Output voltages	Conducting switches
Vdc	$S_5,S_8,S_2,S_{44},S_{88},S_{22}$
2Vdc	$S_8,S_4,S_{44},S_{88},S_{22},S_3$
3Vdc	$S_5,S_8,S_{44},S_{88},S_{22},S_3$
4Vdc	$S_8,S_1,S_{44},S_{88},S_{22},S_3$
5Vdc	$S_8,S_{11},S_{55},S_{88},S_{22},S_3$
6Vdc	$S_8,S_1,S_{44},S_{88},S_{33},S_3$
7Vdc	$S_8,S_1,S_{55},S_{88},S_{33},S_3$
8Vdc	$S_8,S_1,S_{11},S_{88},S_{33},S_3$
0	$S_4,S_8,S_2,S_{44},S_{88},S_{22}$
-Vdc	$S_5,S_7,S_3,S_{11},S_{77},S_{33}$
-2Vdc	$S_1,S_7,S_2,S_{11},S_{77},S_{33}$
-3Vdc	$S_5,S_7,S_2,S_{11},S_{77},S_{33}$
-4Vdc	$S_4,S_7,S_2,S_{11},S_{77},S_{33}$
-5Vdc	$S_4,S_7,S_2,S_{55},S_{77},S_{33}$
-6Vdc	$S_4,S_7,S_2,S_{11},S_{77},S_{22}$
-7Vdc	$S_4,S_7,S_2,S_{55},S_{77},S_{22}$
-8Vdc	$S_4,S_7,S_2,S_{44},S_{77},S_{22}$

A MLI produces a stepped output voltage by additive or subtractive combination of input DC source voltages. Thus the voltage wave form consists of multiple levels with both positive and negative polarities. The proposed topology can be applied in higher voltage application by reducing the problem of voltage stress across the switch.

D. Equations For Hybrid Topology

If N=No. of levels,

Total number of controlled switches required=(N-1) (1)

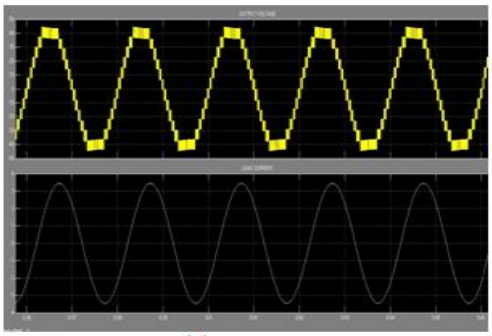
Total numbers of diodes required=(5/4) x (N-1) (2)

Total number of DC sources required=(1/4) x (N-1) (3)

Total number of capacitors required=(1/2) x (N-1) (4)

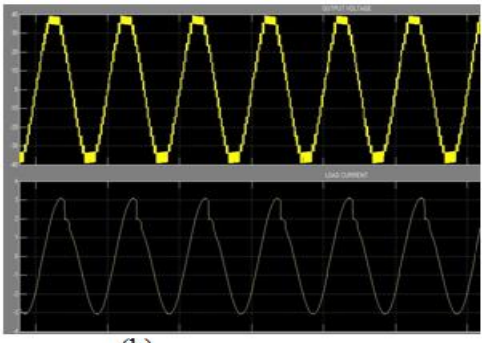
MATLAB SIMULATION

A. MODIFIED TOPOLOGY



(a)

Figure 4: (a) Out put voltage and current for 13 level



(b)

Figure 4: (b)Out put voltage and current for 17 level

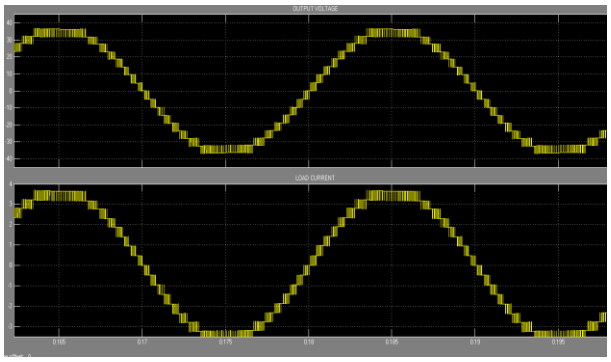
The levels have been simulated in MATLAB 13 version.The output voltage and current are obtained as mentioned in fig.4.As the number of levels increases due to unsymmetrical voltage combination the waveforms become more sinusoidal reducing THD.Load is RL load having R=10Ω and L=25mHwhere carrier frequency is 10KHz.

Table 3: Current THD for 13 level and 17 level

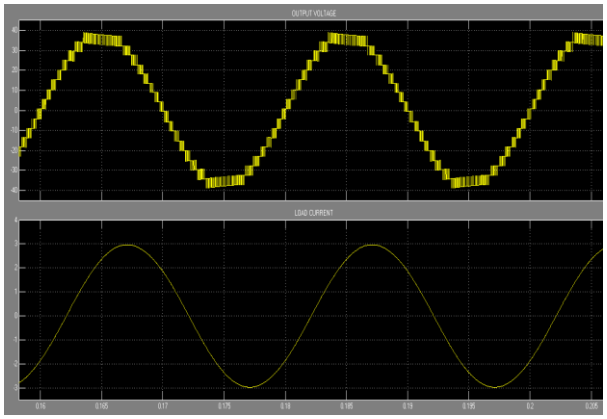
Carrier Frequency in KHz	I_{THD}(13 level)	I_{THD}(17 level)
1	1.91	1.1
3	1.45	0.98
5	1.05	0.91
7	0.94	0.82
10	0.81	0.74

B. Hybrid Topology

Same load is also connected with the hybrid topology in symmetrical configuration .The results are obtained as shown in fig. 5. Fig. 6 and Fig.7 represents the voltage and current THD of the hybrid topology.



(a)



(b)

Figure 5: Output voltage and current in R-Load and Fig.5(b) Output voltage and current in RL-Load

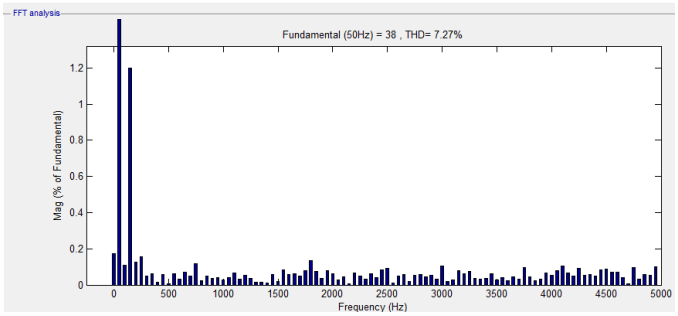


Figure 6 (a): Voltage THD

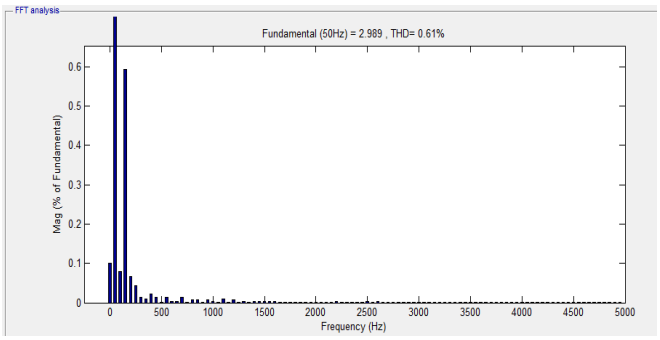


Figure 6 (b): Current THD

Table 4. Carrier Frequencies vs THDs

Carrier frequency in KHz	$V_{O/P}$ in Volt	$I_{O/P}$ in Ampere	V_{THD}	I_{THD}
1	37.29	2.93	7.05	1.61
3	37.5	2.91	7.81	1.34
5	37.67	2.96	8.15	0.96
7	37.68	2.95	9.2	0.76
10	38	2.94	7.27	0.61

The Table 4. represents that with increase in carrier frequencies the output voltage and current remain nearly same but the voltage THD increases and current THD reduces.Therefore more sinusoidal current waveform has been achieved.

Table 5. Modulation Index vs V_{THD}

MODULATION INDEX	V_{THD}
0.6	13.5
0.7	11.7
0.8	9.8
0.9	8.4
1	7.27

It has been observed that in a same carrier frequency the voltage THD reduces as we go on increasing the Modulation Index.

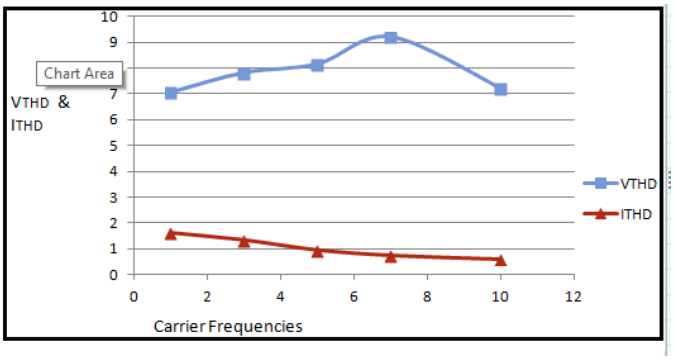


Figure 7 (a): V_{THD} and I_{THD} vs Carrier Frequencies

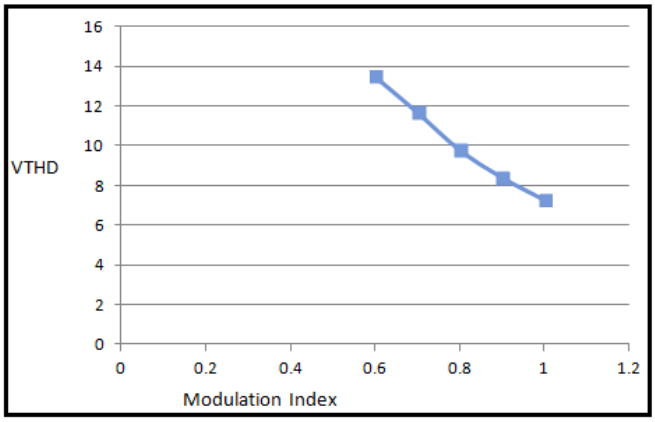


Figure 6 (b): V_{THD} vs Modulation Index

CONCLUSION

In this paper a hybrid topology and again how it can be analyzed has been discussed. The hybrid topology has been compared with other topologies mentioned in the literature survey. It has been concluded that with other existed topologies it has less number of DC sources and semiconductor switches to achieve the same level. Also it has been observed that with increase in levels THD reduces. For same carrier frequency and same load with increase in Modulation index THD also reduces. These features are remarkable in hybrid topology. However this topology can be tested in unsymmetrical condition also.

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