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A Negative Voltage Converter with Wide Operating Voltage Range for Energy Harvesting Applications

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Abstract

In this paper a negative voltage converter (NVC) with wide operating voltage range is presented for full-wave rectifiers required for vibrational energy harvesting. Conventional NVCs adopting the body bias technique can improve the NVC efficiency in the low input voltage region. However, they utilize a simple voltage divider using diode-connected MOS transistors to generate the body bias voltage. The generated body bias voltage varies with the input voltage, making their operating voltage range be limited to 1 V or less. To overcome the problem a beta-multiplier circuit is employed to generate a relatively constant body bias voltage. The proposed NVC is designed in a 0.35-μm CMOS technology and can work with wide input voltage range from 0.6 V to 3.0 V. The simulated power efficiencies are over 85%.

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Keywords: Negative Voltage Converter, Body-Biasing Technique, Full-Wave Rectifier, Beta-Multiplier Circuit, Energy Harvesting.

INTRODUCTION

A full-wave rectifier (FWR) or an AC-DC converter is an essential interface circuit to harvest vibrational energy because the output of a vibrational energy transducer such as piezoelectric (PZT) devices is similar to an ac signal. Recently, active-type FWRs [3-9] have been utilized for energy harvesting applications to reduce diode voltage drop existing in passive-type FWRs [1, 2]. Among the various active FWRs, a two-stage implementation as shown in Fig. 1 has been popularly used [4-9]. The first stage is a negative voltage converter (NVC). This stage cannot charge the load capacitor (C_L) directly because the current direction cannot be controlled. The possible reverse current is blocked by an active diode shown in the second stage of Fig. 1. The active diode is usually composed of a MOSFET switch controlled by a comparator.

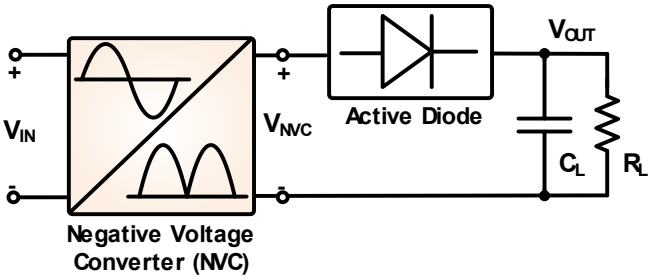


Figure 1: Block diagram of two-stage FWR.

A basic form of the NVC is shown in Fig. 2. It consists of two NMOS and two PMOS transistors and should convert the negative half waves of input sinusoidal waves into positive ones with minimized voltage drop and power consumption. The voltage drop is $V_{SDp}+V_{DSn}$, where V_{SDp} and V_{DSn} are the dropout voltage of PMOS and NMOS transistors respectively. For a low-voltage rectifier, the voltage drop should be minimized for achieving high output voltage efficiency. A straightforward way of lowering the voltage drop is to increase transistor sizes. A more efficient way is to utilize the body bias technique, where the low voltage drop is achieved by applying proper bias voltage to the body terminal of the transistors. By increasing the body

voltage, the threshold voltage and thus, the on-resistance can be reduced, resulting in the low voltage drop.

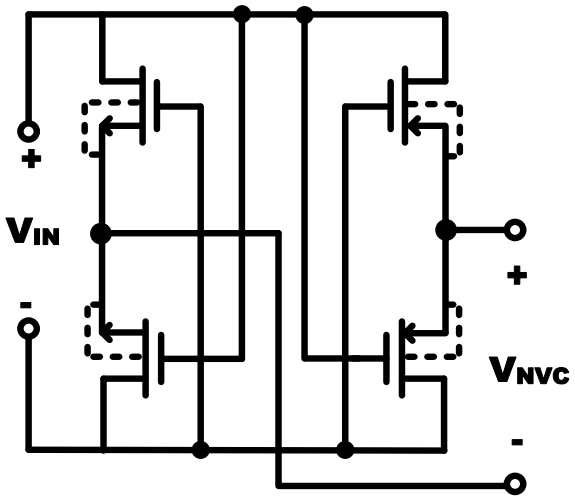


Figure 2: Schematic of basic negative voltage converter.

Several NVCs using the body bias technique have been reported in literatures [7-9]. They use a simple voltage divider using diode-connected MOS transistors to obtain body bias voltages. They show improved performance at low input voltages and extend the operating voltages as low as a few hundred volts. However, their performance becomes degraded as the input voltage increases to more than 1 V. This is because the body bias voltage is not constant but dependent on the input voltage, and thus, it increases with the input voltage, resulting in increased body leakage current. Therefore, their operating voltage ranges are limited to 1 V or less, and their application field is therefore limited.

In this paper we propose a negative voltage converter with wide operating voltage range. The body bias technique is employed to improve the NVC efficiency at low input voltages. The body bias voltage is generated using a beta-multiplier circuit such that it is almost independent of the input voltage. Therefore, comparing with the NVCs in [7-9], the proposed NVC can work with higher input voltages up to 3 V or higher.

PROPOSED NEGATIVE VOLTAGE CONVERTER

The concept of the proposed NVC with body bias technique is shown in Fig. 3. The threshold voltage of a PMOS transistor is usually greater than that of an NMOS transistor. In our design, a 0.35-µm CMOS technology with V_{thn} = 0.63 V and $|V_{thp}|$ = 0.79 V is used. Therefore, the body bias technique with a constant bias voltage of V_{BB} is applied to the PMOS transistors only, and the body of NMOS transistors is connected to ground. The threshold voltage of the PMOS transistor can be expressed as

$$V_{thp} = V_{thp0} + \gamma\left(\sqrt{|-2\phi_F + V_{BB}|} - \sqrt{|-2\phi_F|}\right) \quad (1)$$

where the Fermi potential ϕ_F is positive and the body factor γ is negative for a PMOS transistor [10]. It can be seen from the equation (1) that the magnitude of V_{thp} can be reduced by increasing the body bias voltage V_{BB}. It must be noted that the voltage V_{BB} should be controlled properly such that the body leakage current I_{BB} is negligible.

If the V_{BB} increases to the extent that the body diode is turned on, the body leakage current I_{BB} will also increase sharply.

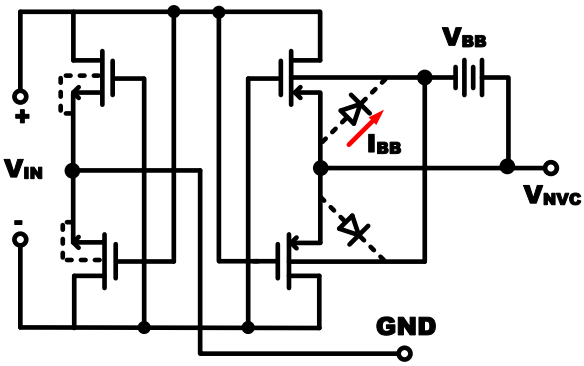


Figure 3: NVC with body bias technique.

Conventional implementation [7-9] of the body bias voltage V_{BB} is to use a simple voltage divider using diode-connected MOS transistors. One of them is shown in Fig. 4. It is powered from the NVC output V_{NVC} which is closely related with the input peak voltage. Therefore, the body bias voltage V_{BB} is not constant but increases with increasing the input voltage. As mentioned before, this could cause a rapid increase in the body leakage current when the input voltage increases beyond a certain voltage.

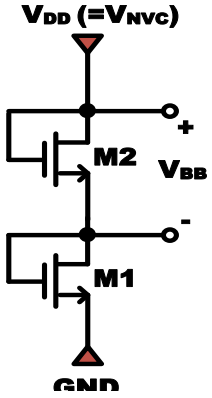


Figure 4: Conventional body bias generation with diode-connected MOSFET voltage divider.

To overcome the problem a supply-independent reference circuit is utilized for the body bias voltage generation. The proposed V_{BB} generator is shown in Fig. 5. It is based on the well-known beta-multiplier structure [10] and includes a start-up circuit [11] consuming no power after startup. To increase the output resistances of the current mirrors, composite transistors (M1-M1a, M2-M2a, M3-M3a, M4-M4a) [12] operating in subthreshold region are employed. By using the composite transistors, the output impedance of the current mirror becomes comparable to that of a cascade current mirror without affecting its output voltage swing and without requiring any additional power dissipation. The supply voltage dependence of the output voltage $V_{BB}(=V_{DD}-V_{OUT})$ and the output current I_{OUT} with respect to power supply is shown in Fig. 6. The simulated V_{BB} is 475 mV when the input voltage is greater than 0.6 V. The V_{DD} sensitivities of V_{BB} and I_{OUT} are 1.14 mV/V (0.24 %/V) and 66 pA/V (2.9 %/V) respectively.

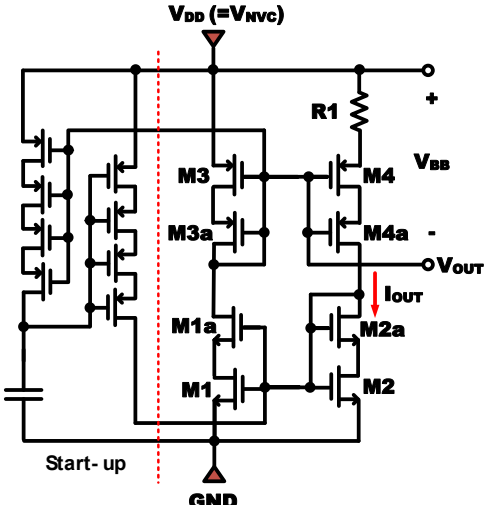


Figure 5: Proposed body bias generation with beta-multiplier reference circuit.

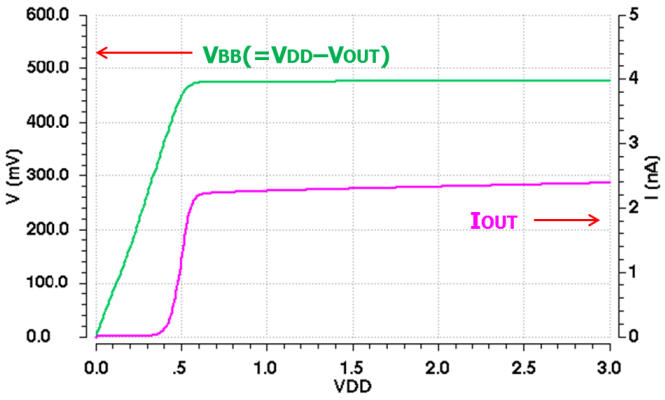
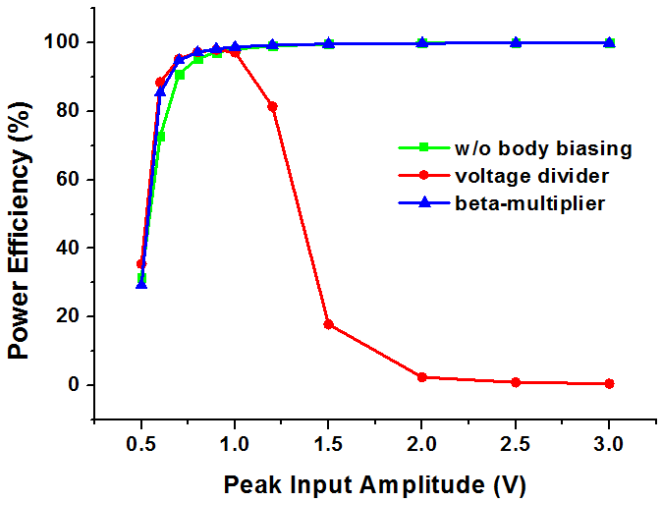


Figure 6: Supply voltage dependence of the output voltage and current.

SIMULATION RESULTS

The proposed NVC is compared through extensive simulation with the simple NVC without body biasing in Fig. 2 and the conventional NVC with body biasing using the simple voltage divider in Fig. 4. The NVCs have been simulated using a 0.35-µm CMOS process. The default input frequency is 100 Hz and a load resistance of 100 kΩ is used.

The simulated power efficiencies for different input peak voltages are shown in Fig. 7. It can be seen from the magnified view that the efficiencies in the low input voltage region (less than 1.0 V) are improved in the NVCs using body bias technique. As expected, the power efficiency of the NVC using the voltage divider decreases sharply beyond a certain input voltage around 1.0 V. However, the proposed NVC shows almost the same efficiencies in the higher input voltage region (from 1.0 V to 3.0 V). The detailed body bias voltage and leakage current comparisons of the two NVCs using body bias technique can be seen in Fig. 8 and 9. The average and peak body voltages, $V_{BB,avr}$ and $V_{BB,peak}$ in the conventional NVC using a simple voltage divider increases with increasing the input voltage. This results in the considerable and unacceptable increase in the average or peak body leakage currents as can be seen in Fig. 9. In the proposed NVC, the average and peak body bias voltages are almost constant when the input voltage is greater than 1.0 V. Therefore, the body leakage currents are well controlled to low levels which results in higher efficiencies. It has been verified that the similar results are achieved with different load resistances.



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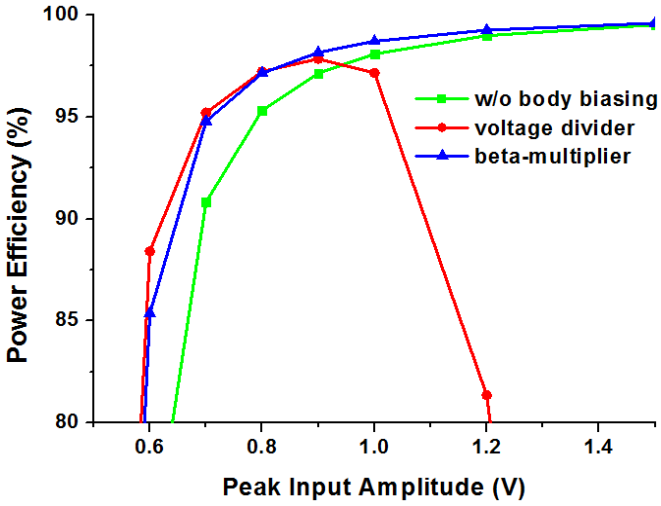
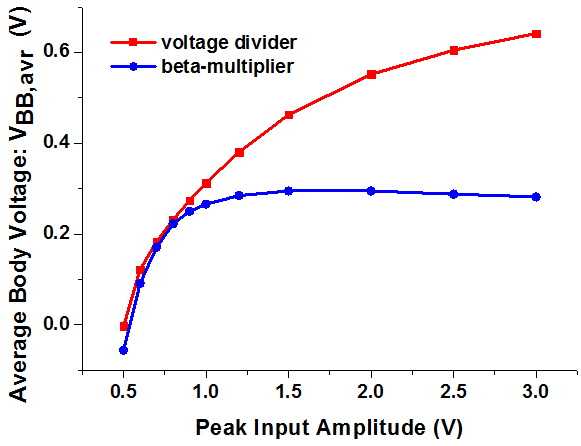


(b)

Figure 7: (a) Simulated power efficiencies versus input voltage with f = 100 Hz, R_L = 100 kΩ, (b) Magnified view.



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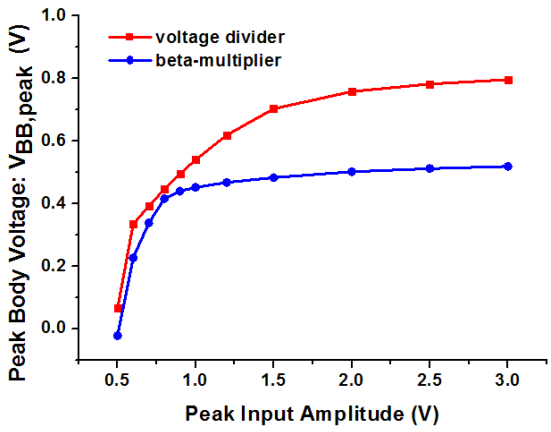
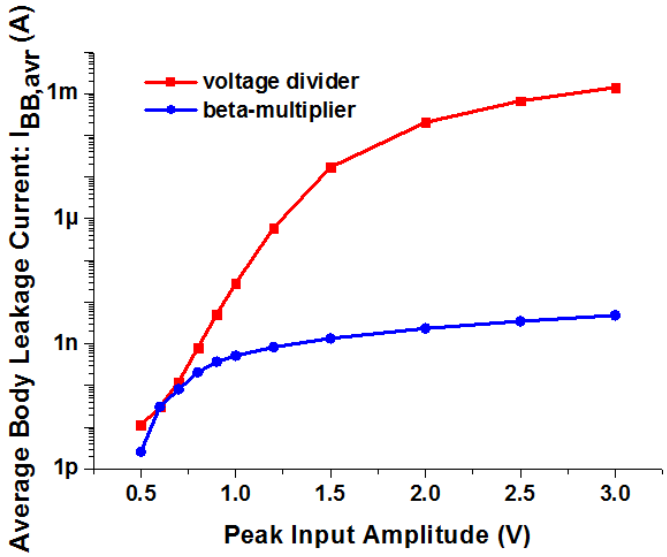


(b)

Figure 8: (a) Average body voltage, (b) Peak body voltage versus input voltage.



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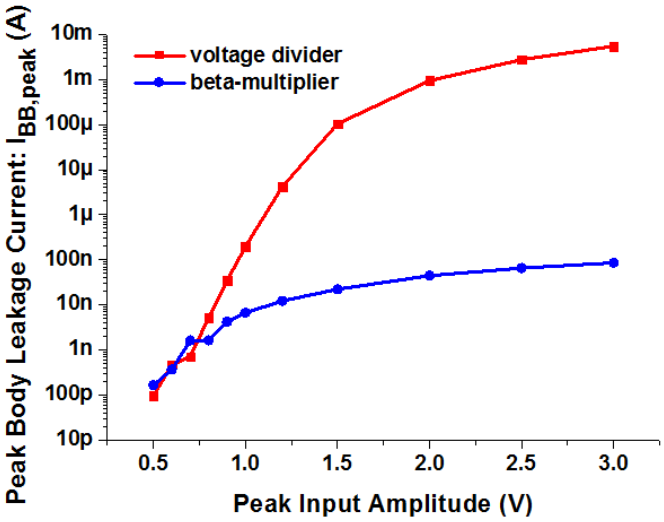


Figure 9: (a) Average body leakage current, (b) Peak body leakage current versus input voltage.

Fig. 10 shows the simulated output waveforms with a sinusoidal 0.8 V input at 100 Hz and loaded with a 100 kΩ resistor. It can be seen from the magnified view in Fig. 11 (a) that the voltage efficiencies of the NVCs using body bias technique are higher than that of the simple NVC without body biasing. However, when the input voltage is increased to 1.2 V, the voltage efficiency of the NVC using a simple voltage divider becomes smaller than that of the simple NVC. The proposed NVC using a beta-multiplier circuit has the highest voltage efficiency as can be seen in Fig. 11 (b).

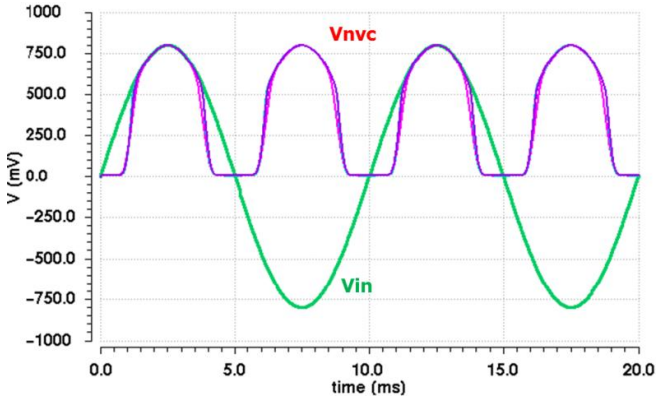
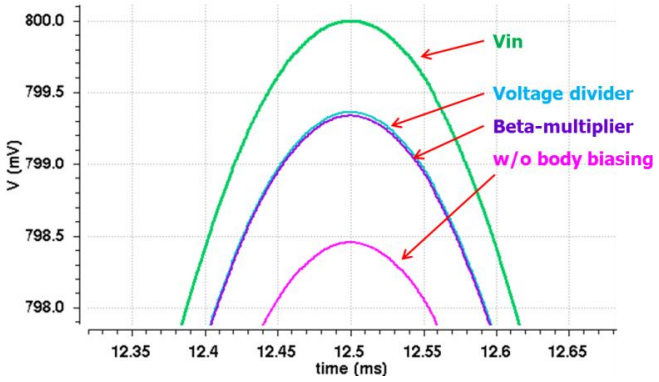


Figure 10: NVC output waveforms with a sinusoidal 0.8 V input at 100 Hz and loaded with a 100 kΩ resistor.



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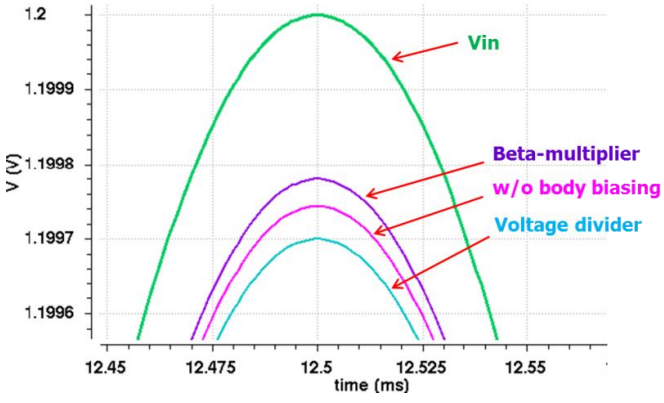

(b)

Figure 11: Magnified view of the output waveforms (a) with a sinusoidal 0.8 V input, (b) with a sinusoidal 1.2 V input.

CONCLUSION

In this paper, a negative voltage converter with wide operating voltage range for energy harvesting applications is proposed. To improve the NVC efficiency in the low input voltage region the body bias technique using a beta-multiplier circuit is employed. Owing to the relatively constant body bias voltage, the proposed NVC designed in a 0.35-μm CMOS technology can work with input voltage range from 0.6 V to 3.0 V. The power efficiencies are over 85%. The proposed NVC is suitable for applications where energy harvesting is required for wide voltage range.

ACKNOWLEDGEMENT

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