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Intelligent Sensor Module For Wireless Sensor Network (WSN) in Electrical Power Management Applications

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Abstract

The need in the industry for more efficient control systems in conjunction with the latest advances in digital systems and wireless communication has stimulated in recent years research into advanced monitoring and supervisory systems. In this paper we present a proposal of intelligent sensor module for use as a node in a Wireless Sensor Network (WSN). This module is capable of processing the true RMS (Root-Mean Square) voltage, and transmitting the value along the network. To do this, the design makes use of a COordinate Rotation DIgital Computer (CORDIC) implemented on a FPGA (Xilinx SPARTAN 3E 1600). Thanks to this implementation, the prototype is able to process electrical signals in real time with a minimalist architecture of high performance and low energy consumption. The effectiveness of the proposed designs is assessed through FPGA (Field-Programmable Gate Array) implementations and error simulations. A test bench has been created to validate the basic functions of the proposed intelligent sensor node.

Keywords: Cordic, embedded system, intelligent sensor, real-time, true RMS.

INTRODUCTION

Wireless sensor networks (WSNs) are one of the latest technology trends, and have gained in popularity thanks to its communication structure, ubiquitous computing, versatility and relative low cost. These networks are composed of a set of autonomous elements (nodes) interconnected wirelessly. Nodes have specific sensors, and communication capability. They form ad-hoc networks (each node can re-send data to others) without pre-established physical infrastructure or central administration [1].

Nodes in the network have limited resources, both in processing capacity and in operating energy (batteries) [2]. These characteristics limit the processing capacity of the node, and increase the amount of information to be transmitted. An ideal solution is to achieve an intelligent node with high processing capacity, low hardware and low power consumption.

On the other hand, the WSN as a tool for energy management offers several advantages:

- Low installation and maintenance costs.
- Easy replacement and upgrade.
- High reliability given its natural redundancy.

In particular, these WSNs measure electrical parameters at different points in the electrical network, and with these data the electrical management can be improved in terms of:

- Energy consumption.
- Energy generation.
- Transport of energy.
- Performance in facilities.
- Power quality.
- Comfort.
- Environmental care.

This research focuses on the voltage sensor node. However, the basic theory is implemented in other intelligent sensors in development by the research group. The goal is to have a minimalist sensor of true RMS voltage. For this we propose an embedded system supported by FPGA, which performs the processing through a CORDIC.

CORDIC is an iterative algorithm for calculating hyperbolic and trigonometric functions [3], and for computing inverse trigonometric functions [4]. It is particularly suited to hardware implementations because it does not require any multiplies. Its importance is high in embedded systems because most processing algorithms require such operations [5]. The algorithm was originally developed as a digital solution for real-time navigation [6, 7]. This allows to develop embedded systems for specific applications, in particular with low complexity and high accuracy characteristics, key elements on hardware implementation [8, 9, 10].

There are two modes of CORDIC: rotation and vectoring [11, 12]. The vector is rotated by a desired angle in rotation mode, whereas the vector is aligned with X-axis in vectoring mode. In this research we use the rotation mode for the synthesis of

functions. Fixed-angle-rotation operation is widely used in signal processing [13]. Various CORDIC designs have been proposed for uniform rotation of vectors through specified angles with modest use of resources (Look-Up Tables or LUTs, and Flip-Flops) [14, 4, 15]. In many cases the algorithms use pipeline to allow different functional units to operate concurrently [16].

Thinking about simplifying the implementation hardware, CORDIC is an iterative algorithm which requires shift and addition operations. One of the main uses of the algorithm is the hardware realization of the sine and cosine of an angle. From these functions it is possible to determine operations like multiplication, division, hyperbolic, exponential, logarithm and square root [7]. Because FPGA is a high-speed programmable device, it has been widely used to realise CORDIC based algorithms [17]. Their joint use has been particularly important in embedded systems and robotics, applications which guarantees an efficient system for calculating angles and distances [8].

The following part of the paper is arranged in this way. Section 2 presents preliminary concepts and problem formulation. Section 3 illustrates the methodology based on CORDIC to estimate the effective value of the signal and the general architecture of the intelligent module. Section 4 we present the preliminary results. And finally, in Section 5, we present our conclusions.

PROBLEM FORMULATION

The voltage at a given node in the electric power network can be affected by nonlinear loads that generate harmonic content due to the circulation of non-sinusoidal currents. In any case, it is considered that the signal is not sinusoidal, but it is periodic.

Periodic waves, such as the case of grid voltage $V(t)$, have frequency components that are multiple integers of some fundamental frequency. This voltage signal can be expressed as the sum of the fundamental, its harmonics, and some DC value (V_0, equation 1).

$$V(t) = V_0 + \sum_{h=1}^{N} V_h \, sin[h\omega t + \theta_h] \quad (1)$$

Equation 2 shows how to find the RMS value of a voltage waveform, where the RMS value of each of the harmonics, V_h, is known.

$$V_{RMS} = \sqrt{\sum_{h=1}^{N} (V_h)^2} \quad (2)$$

Many voltage measuring devices assume sinusoidal waveform, and calculate the value from the peak of the signal. Others calculate an average value. In both cases the reading is only correct if the signal is sine, and is erroneous in the cases of square, triangular, or periodic waves with harmonic content (general case of the power grid). Therefore, the calculation from equation 2 is called true RMS, and is expected in a good measurement equipment.

It is proposed to perform the square root calculation and the exponentiation, and even the approximation of the signal sampled between sample and sample, from the calculation of sines and cosines using the CORDIC algorithm. To determine the sine or cosine of an angle it is necessary to find the *x* and *y* coordinates of its vector in the unit circle (Figure-1). CORDIC begins with vector V_0. In the first iteration, this vector is rotated 45 degrees counter-clockwise to get the vector V_1. Successive iterations rotate the vector in one or the other direction by size-decreasing steps until it reaches the desired angle. Every iteration calculates the rotation multiplying the vector *n* with the rotation matrix R_i (equation 3).

$$V_n = R_i * V_{i\text{-}n} \quad (3)$$

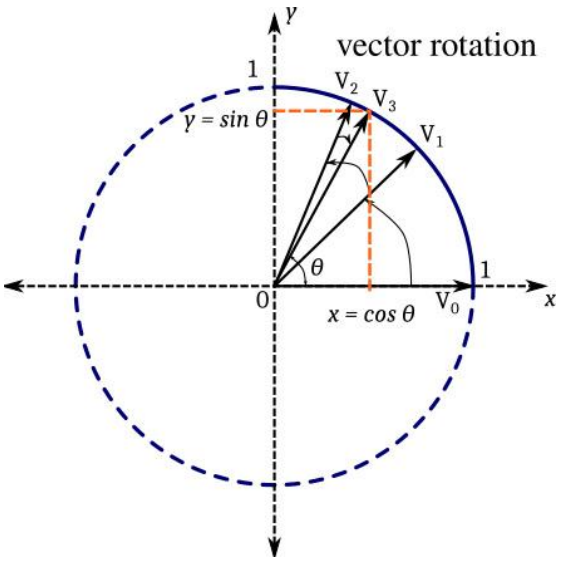

Figure -1. CORDIC vector rotation

Where the rotation matrix is given by (equation 4):

$$R_i = [cos\ \theta_i \quad -sin\ \theta_i;\ sin\ \theta_i \quad cos\ \theta_i] \quad (4)$$

The direction of rotation is defined according to the error with respect to the desired vector. Knowing further that (equation 5):

$$cos\theta = \frac{1}{\sqrt{1+tan^2\theta}} \quad , \quad sin\theta = \frac{tan\theta}{\sqrt{1+tan^2\theta}} \quad (5)$$

After some iterations the angle of the vector will get close enough to θ.

Our research seeks to implement this strategy for the development of embedded systems dedicated to the real time processing of electric power quality. For this, we evaluate the performance of three CORDIC cores:

- Trapezoidal fit between samples.
- Calculation of the square, and
- Calculation of the square root.

This embedded system is attached to a communication module, to a central control unit and an electric power supply system to form the intelligent sensor node.

MATERIALS AND METHODS

Figure-2 shows the proposed architecture for the node. The control unit is in charge of the activation of each one of the units of the node, determines when sensing signals and when transmitting them. It also controls the information recorded in the external memory and monitors the battery level (power unit).

The first block performs the conditioning of the input signal. There is a sub-block that is responsible for adjusting the voltage level using a resistive divider according to the specifications of the ADC (Analog-to-Digital Converter). This signal is then discretized to 14 bits with the ADC (Linear Technology LTC-1407-1A). This block also includes a zero crossing sensor circuit for calculating the period. This circuit is basically a voltage comparator synchronized with the clock signal.

A fundamental aspect in the design of the node is its power consumption. Power consumption must be minimized by reducing the level of processing and the transmission of information. In both aspects, the processing of information with the CORDIC is fundamental. In addition, both the data collection and its transmission contemplate an event-driven architecture, with a control algorithm that determines when to sense and when to transmit.

Intelligent sensor module

The CORDIC was implemented by hardware on a Xilinx SPARTAN 3E 1600 FPGA. The block diagram shown in Figure-3 depicts the steps to be followed in the computation of true RMS. The system consists of three functional blocks: Pre-process, Iterations and Post-process.

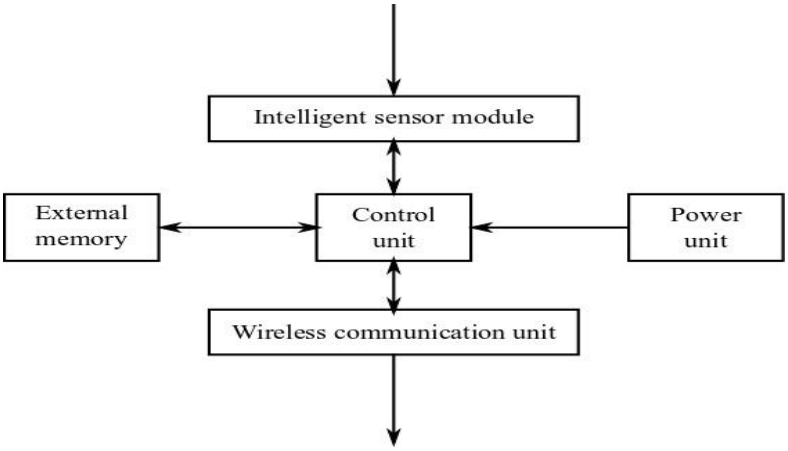

Figure-2. Sensor node architecture

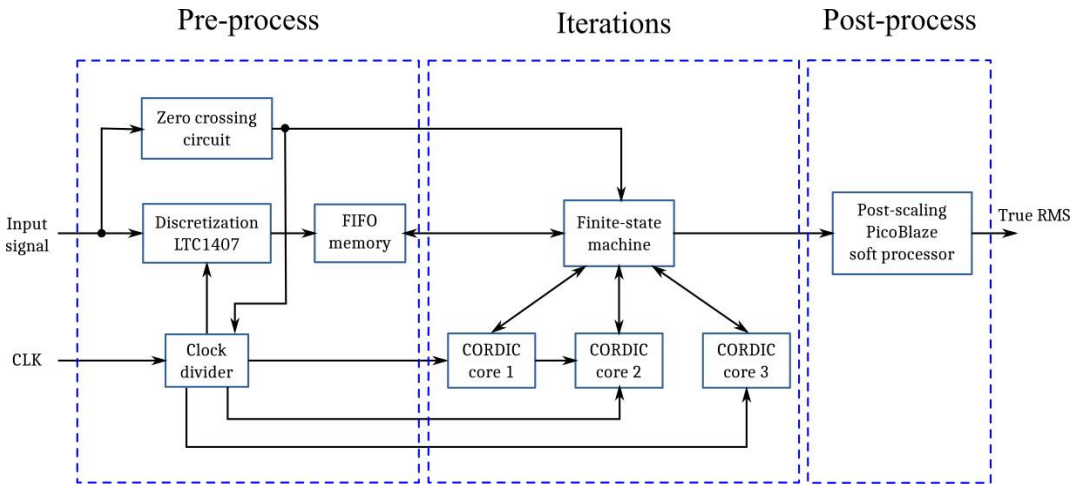

Figure-3. Intelligent sensor module architecture

The second block revolves around a Finite-State Machine (FSM) and the three CORDIC cores. In this block the trapezoidal estimation of the samples is performed, and the calculation of square and square root functions, one in each of the CORDIC cores.

In the case of the square root, we will think that the input value is given by equation 6 (the *a* is the input value). The *a* * *k*^2 is within the appropriate range for the CORDIC. We set *k* to 2 because the power of 2 can be realized by shift operation (ideal case for fixed point).

$$k\ \mathrm{sqrt}(a) = \mathrm{sqrt}(a*k\hat{}2) \quad (6)$$

Figure-4 shows a performance comparison. Functions are plotted for a relatively large sampling interval (20 us) to highlight their differences. The blue and red lines show the square root and the CORDIC square root, respectively. For short sampling intervals and/or larger intervals the two lines almost become one. Something similar is implemented for cases of trapezoidal interpolation and square.

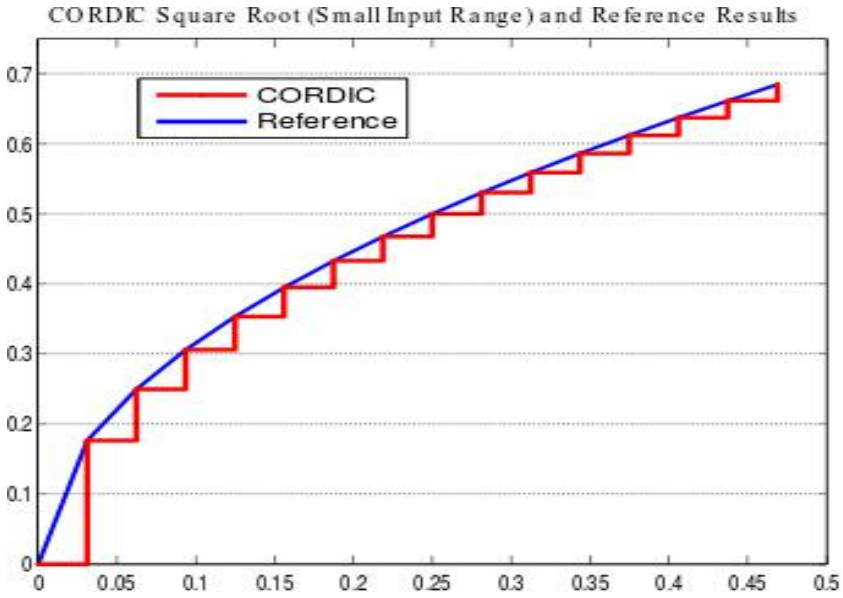

Figure-4. Computer simulation vs CORDIC implementation result of the square root function

Table-1. Comparison of performance against different test signals

No data	Frequency [Hz]	Signal	Peak Voltage [V]	Prototype Reading [V]	Fluke 87 Reading [V]	Expected Value [V]	Error Prototype	Error Fluke 87
0	3061	sine	10	7,300	6,75	7,07	3,24%	5%
1	3061	triangular	10	5,976	5,76	5,77	3,51%	0%
2	3061	square	10	10,120	9,60	10,00	1,20%	4%
3	0	dc	10	10,230	9,80	10,00	2,30%	2%
4	60	sine	10	7,270	6,75	7,07	2,81%	5%
5	60	triangular	10	5,930	5,70	5,77	2,71%	1%
6	60	square	10	10,120	9,60	10,00	1,20%	4%
7	0	dc	10	10,223	9,80	10,00	2,23%	2%
8	60	sine	5	3,632	3,40	3,54	2,73%	4%
9	60	triangular	5	2,950	2,76	2,89	2,19%	4%
10	60	square	5	5,300	4,80	5,00	6,00%	4%
11	0	dc	5	5,200	4,98	5,00	4,00%	0%
12	4549	sine	5	3,290	3,10	3,54	6,94%	12%
13	4529	sine	10	7,310	6,68	7,07	3,38%	6%
14	4529	triangular	5	3,024	2,59	2,89	4,75%	10%
15	1000	square	5	5,017	4,55	5,00	0,34%	9%
16	4529	square	5	5,100	4,27	5,00	2,00%	15%
17	12930	sine	6,24	4,197	3,98	4,41	4,88%	10%
18	12930	triangular	6,24	3,390	3,28	3,60	5,90%	9%
19	12930	square	6,24	6,100	5,38	6,24	2,24%	14%
20	20000	sine	7,2	5,040	4,96	5,09	1,01%	3%
21	20000	triangular	7,2	4,178	4,09	4,16	0,51%	2%
22	20000	square	7,2	7,030	6,57	7,20	2,36%	9%

The last block is formed by a PicoBlaze as processor embedded in the FPGA. This processor is responsible for the scaling of the output and its presentation on a LCD (Liquid-Crystal Display).

Wireless communication unit

The communication is coordinated by a small IoT (Internet of Things) unit. We use a SoC (System On a Chip) from Espressif Systems with the Tensilica Xtensa LX106 core. The communication scheme uses the MQTT protocol. The data collected by the sensor are delivered through the network to a remote unit (broker) for online analysis and control. The sensor node, its architecture and its communication protocol were specifically designed with fault tolerance, adaptability and network self-organization criteria. These design criteria guarantee a fast and robust operation in real environments, and a long operating time.

The network structure is star type (single point-to-multipoint). The broker can send or receive messages to the nodes, but they can not communicate with each other. This architecture, in addition to simple, significantly reduces the power consumption of the nodes. Also, allows low latency communications between the remote node and the broker.

RESULTS AND DISCUSSION

The performance tests sought to determine the capability and versatility of the prototype node, but particularly of the module that processes the true RMS. Therefore, we perform measurements on a set of known test signals, and we contrast the results against a calibrated laboratory equipment. The selected reference device is the Fluke 87, true RMS capable device. The reference signals are:

- Sine signal with frequencies from 1 to 20 kHz
- Square signal with frequencies from 1 to 20 kHz
- Triangular signal with frequencies from 1 to 20 kHz
- Constant DC signal of different values

Table 1 shows the results for 23 of these tests. The average error reached by the prototype against the references was 3.1%, while the Fluke 87 registered an average error of 5.8% with the same data.

The computational cost tests sought to determine the savings in prototype resources versus a traditional FPGA implementation without the use of CORDIC. In the initial tests we were able to determine a 31% reduction in No. of Slice LUTs (LookUp Tables), and 11% in No. of Slice Registers. In addition, the algorithm can be executed at a higher frequency. This reduction in processing is reflected directly in a reduction in energy consumption compared to other solutions on FPGA.

CONCLUSIONS

This paper proposes the design of an intelligent sensor node for a wireless sensor network. The objective of the node is, in this first stage, to estimate the true effective value of a voltage signal, using a minimum level of processing (and therefore a low energy consumption) for signals that are expected to have harmonic distortion. To meet these criteria, we implemented a CORDIC algorithm in an embedded system supported by FPGA. This algorithm is used for the calculation of: trapezoidal fit between samples, calculation of the square, and calculation of the square root. The use of the CORDIC reported in the laboratory a reduction in the computational complexity of at least 30%, with a functional performance close to that identified in industrial equipment. The structure of the algorithm is simple and flexible, allowing its adaptation in a large number of applications of energy quality processing, in particular in power factor active correctors. Laboratory tests on a bench test created for these sensors corroborate not only the high performance of the network, but also an equivalent reduction in total energy consumption.

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