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Design and Implementation of Asynchronous 8-bit Microprocessor

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ABSTRACT

A delay-insensitive asynchronous design methodology, named NULL Convention Logic (NCL), is one of mainstream asynchronous design techniques for low-power robust circuit operation. It offers many advantages over synchronous circuit design having scaling issues in nanometer region such as severe process variations, short channel effects, aging effects, and etc. Therefore, this paper proposes a new design methodology to convert synchronous circuits into NCL circuits in RTL (register transfer level) and a new interfacing block to connect NCL circuits to synchronous circuits/memories or synchronous circuits/memories to NCL circuits. In this paper, the proposed methodology has been evaluated by an 8051 microprocessor designed using a standard 0.35um CMOS technology, and the experimental results show that the proposed asynchronous 8051 microprocessor reduces power consumption by 40% compared with a synchronous 8051 microprocessor.

Keywords: Asynchronous Circuit, Microprocessor, 8051, Null Convention Logic

INTRODUCTION

Currently, most digital circuits have been designed by a synchronous design methodology. However, fully-synchronous digital systems have the weakness of high power consumption because clock distribution over whole synchronous circuits is a large source of power consumption. Especially, the conventional synchronous design circuits cannot satisfy the timing requirement of the low voltage digital systems, but also can generate wrong outputs under the influence of scaling issues in nanometer region such as severe process variations, short channel effects, aging effects, and etc.

Therefore, in the reliable ultra-low power design, asynchronous circuits have recently been re-considered as a solution for the scaling issues, and Null Convention Logic (NCL) is one of the promising delay-insensitive asynchronous circuit design methodologies. It has many advantages of inherent robustness, power consumption, and easy design reuses [1][2].

Despite the recent promising progress of the NCL design methodology, NCL implementation at very large digital circuits has not been achieved. The main reasons are that the NCL circuits cannot easily convert synchronous circuits into NCL circuits in RTL (register transfer level). Also, it has not been proposed for a new interfacing block to connect NCL circuits to synchronous circuits/memories or synchronous circuits/memories to NCL circuits.
Therefore, this paper proposes a new design methodology to convert synchronous circuits into NCL circuits in RTL (register transfer level) and a new interfacing block to connect NCL circuits to synchronous circuits/memories or synchronous circuits/memories to NCL circuits. In this paper, a new asynchronous 8051 microprocessor based on the NCL design methodology has been designed and implemented in a standard 0.35um CMOS technology.

8051 MICROPROCESSOR

A conventional synchronous 8051 microprocessor contains over 60,000 transistors, 4K bytes ROM, 128 bytes of internal RAM, 32 I/O ports, serial ports, interrupts and two timers and counters [3]. Figure 1 shows the 8051 architecture. In Figure 1, additional circuitries have been connected to memories (external RAMs for data storage and ROMs for program storage) and ports, and internal RAMs, in/out ports, two timers, two counters and serial interface unit are built in the 8051. The microprocessor gives the satisfactory performance in small systems, but suffers from memory limitation because only 64KB memory is used for program storage. The SFR registers are located in the internal memory (address range 80H to FFH). Each SFR has a specific function and is accessed as same as normal internal RAMs are accessed [3].

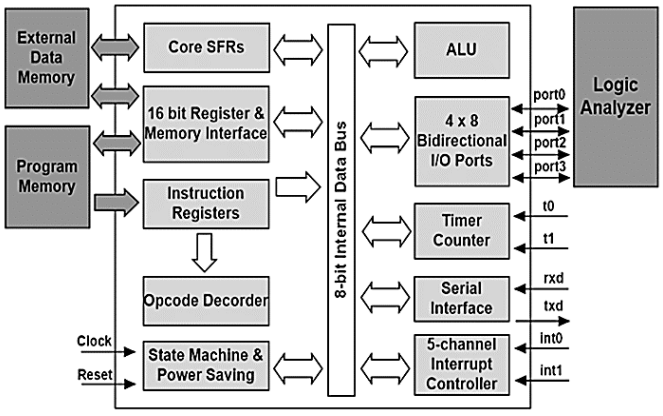

Figure 1: 8051 Architecture

In this paper, the proposed 8051 microprocessor uses the mc8051 core developed from Oregano systems. The 8051 IP core is a fully synchronous design. There is a single clock signal that controls the clock input of every storage element.

The clock signal is not fed into any combinatorial element. The interrupt input lines are synchronized with the global clock signal using a standard two-level synchronization stage because they may be driven by external circuitry with another clock [4]. The original microprocessor design offers only 2 timer/counter units, one serial interface, and two external interrupt sources. The 8051 IP-core offers the capability to generate up to 256 of these units by simply changing a VHDL constant's value. Figure 2 shows the block diagram of the MC8051. The core itself is made up of the submodules timer, counter, ALU, serial interface unit, and control block. RAM or ROM blocks are most often generated depending on the selected target technology. Table I shows the core specification of the 8051 microprocessor [4].

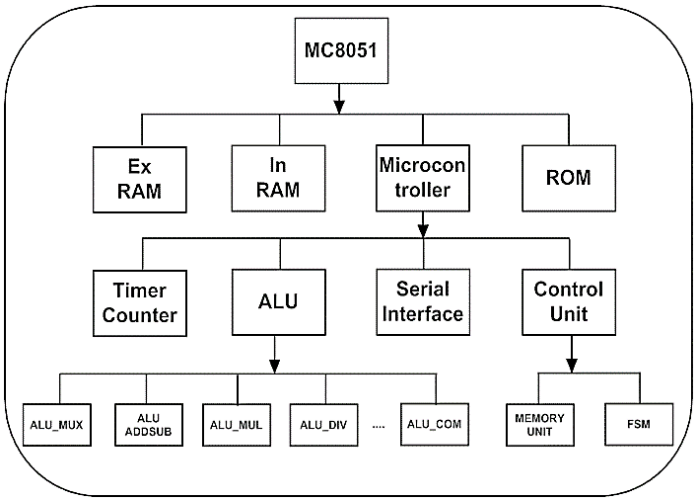

Figure 2: 8051 Block diagram

Table 1: 8051 core specification

8051 Core Specification	
8-bit CPU optimized control applications	
64K Program Memory address space	
64K Data Memory address space	
Up to 4K bytes of on-chip Program Memory	
128 bytes of on-chip Data RAM	
32 bi-directional and individually addressable I/O lines	
Two 16-bit timer/counters	
6-source/5vector interrupt structure	
Supply Voltage(V)	3
Speed(MHz)	10~15
Power(W)	9.09E-03

ASYNCHRONOUS DESIGN METHODOLOGY

NULL CONVENTION LOGIC (NCL) :

In the reliable ultra-low power design, asynchronous circuits have recently been re-considered as a solution for scaling issues [5]. Null Convention Logic (NCL) is one of the promising delay-insensitive asynchronous circuit design methodologies [6]-[10]. NCL circuits utilize threshold gates with hysteresis to maintain delay insensitivity. NCL uses delay-insensitive codes for data communication, alternating between set and reset phases. NCL uses threshold gates with hysteresis for its logic elements. One type of threshold gate is the THmn gate as shown in Fig. 3 (a), where $1 \leq m \leq n$. A THmn gate means that at least m of the n inputs has to be asserted before the output will become asserted. For example, Figure 3 (b) shows TH34w2 threshold gate. Threshold gate inputs and outputs can be in of two states, DATA or NULL [5].

A threshold gate starting with its output in a NULL state will remain in the NULL state until the specified numbers of inputs are placed in the DATA state. Once the gate reaches the DATA state, it remains in this state until all of the inputs return to the NULL state. A dual-rail signal, D, consists of two wires, D0 and D1, which may assume any value from the set DATA0, DATA1, NULL. The DATA0 state (D0 = 1, D1 = 0) corresponds to logic zero, the DATA1 state (D0 = 0, Dl = 1) corresponds to logic one, and the NULL state (D0 = 0, D1 = 0) corresponds to the empty set meaning that the value of D is not yet available. The two rails are mutually exclusive, so that both rails can never be asserted simultaneously; this state is defined as an illegal state as shown in Table 2. Figure 4 (a) presents the NCL pipeline structure based on local handshaking flow, and Figure 4 (b) the DATA/NULL cycle in the NCL pipeline structure.

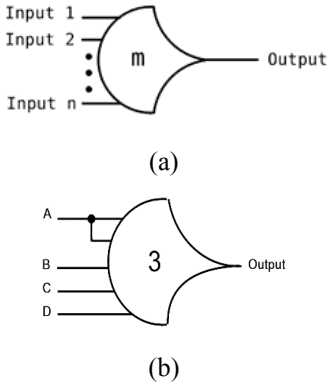

Figure 3: (a) Thmn NCL gate symbol, (b)TH34w2 threshold gate: Z = AB + AC + AD + BCD

Table 2: Dual-rail encoding

	DATA 0	DATA 1	NULL	Illegal
Rail0	1	0	0	1
Rail1	0	1	0	1

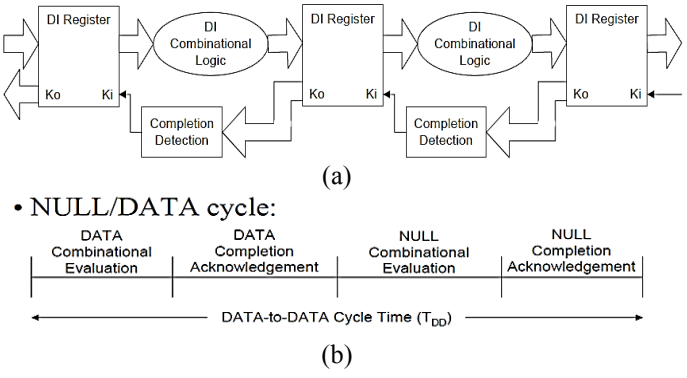

Figure 4: (a) NCL pipeline structure, (b) DATA/NULL cycle

INTERFACING BLOCK BETWEEN SYNCHRONOUS AND ASYNCHRONOUS CIRCUITS :

It is desirable to change main blocks of synchronous systems to asynchronous blocks except critical blocks like internal memories. Moreover, if the interfacing block is deployed in the primary inputs and outputs, it is possible to verify the entire NCL circuit using conventional single-rail signals instead of using the NCL dual-rail signals of DATA0 and DATA1.

Figure 5 shows the block diagram of the interfacing block, and it is divided in two blocks of asynchronous-to-synchronous block and synchronous-to-asynchronous block controlled by clock- gating method. In order to interface between a synchronous block and NCL block, a digital value like "0" or "1" must be translated into dual-rail value like DATA0 or DATA1.

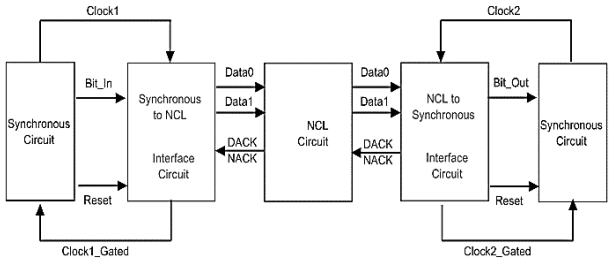

Figure 5: Interfacing between synchronous and asynchronous circuits

ASYNCHRONOUS MICROPROCESSOR DESIGN :

Our design methodology converts conventional synchronous digital design into dual-rail asynchronous designs using NCL logics. The specification level is a register-transfer level, which means that the designer is responsible for creating both data-path (registers and compute blocks) and control (finite state machines, sequencers). The proposed asynchronous 8051 has been designed using Verilog language in RTL, and a commercial synthesis tool is used to synthesize to a netlist of D-flip-flops, latches, combinational logic, and special gates known by the toolset. Our design methodology converts single-rail synchronous netlists into dual-rail asynchronous NCL netlists, and then generates the acknowledge network to make the NCL pipeline structure. The generated gate level netlists can be simulated in a Verilog simulator or serve as the input netlists to a VLSI environment for transistor level simulation. Performance optimization via latch movement to balance data/acks delays is supported.

Table 3 presents the translation of the 8x8 NCL multiplier Verilog code using our methodology. As shown in Table 3, the 8x8 NCL multiplier Verilog code only uses the NCL standard cell gates.

EXPERIMENTAL RESULTS

The simulation Firstly, the proposed 8051 design has been implemented using Xilinx FPGA(Virtex5). Figure 6 shows the waveform of 8051 counters, and the TL register and TH register counts and increases 1 bit.

Table 3: NCL Verilog Code.

8x8 NCL multiplier Verilog code
module ncl_mul8x8 (t_a, f_a, t_b, f_b, t_y, f_y, ackout, ackin, reset);
input reset ;
input ackin ;
output ackout ;
output [15:0] f_y ;
output [15:0] t_y ;
input [7:0] f_b ;
input [7:0] t_b ;
input [7:0] f_a ;
input [7:0] t_a ;
…
th23 \mult_21/S3_2_6_U_U_2 (.a (\f_mult_21/ab[1][7]) , .b (\f_mult_21/ab[2][6]) , .c (\f_mult_21/CARRYB[1][6]) , .y (\f_mult_21/CARRYB[2][6]));
th34w2 \mult_21/S2_3_3_U_U_0 (.a (\t_mult_21/CARRYB[3][3]) , .b (\f_mult_21/SUMB[2][4]) , .c (\f_mult_21/ab[3][3]) , .d (\f_mult_21/CARRYB[2][3]) , .y (\f_mult_21/SUMB[3][3]));
th22 U105_U_0 (.y (t_n13) , .b (t_n16) , .a (t_n15));
th44 cgate9 (.a (acknet40) , .b (acknet39) , .c (acknet38) , .d (acknet37) , .y (acknet41));
thand0 U129_U (.y (f_n29) , .d (f_n25) , .c (t_n27) , .b (t_n25) , .a (f_n27));
th24comp U106_U (.y (t_v_product[14]) , .d (f_n17) , .c (f_n15) , .b (t_n15) , .a (t_n17));
…
endmodule

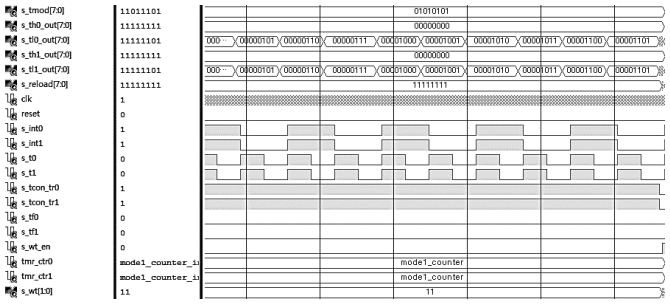

Figure 6: Simulation result of 8051 counter

Figure 7 shows the led on/off operation using counter's overflag: when the led is on, the output Port 1 value is "00000010"; when the led is off, the output Port 1 value is "00000000".

Figure 8 shows the 8x8 NCL multiplier function waveform. The first input of DATA0 and DATA1 is "83", "7C", and the another input of DATA0 and DATA1 is "16", "E9", respectively. The output of DATA1 is "70DC". Figure 8 presents the implementation of NCL ALU using Xilinx FPGA.

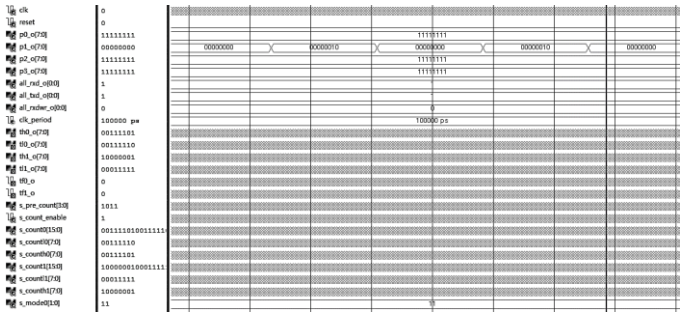

Figure 7: Simulation result of LEDs by a counter's overflag

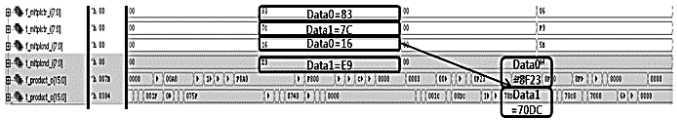

Figure 8: Simulation result of an 8x8 multiplier.

As shown in Figure 9, the results on a logic analyzer show a correct function waveform in a Xilinx board level test.

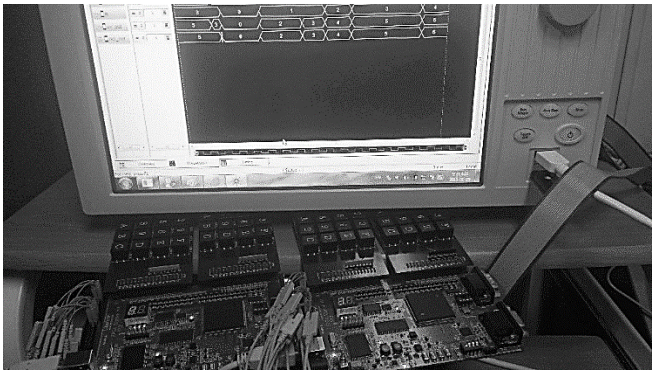

Figure 9: Xilinx FPGA implementation of NCL 8051

Secondly, the proposed asynchronous design methodology evaluated using the proposed microprocessor designed in a 0.35um standard CMOS process technology. Figure 10 shows the die photo of the proposed 8051 design. The 8051 size is 3.3mm x 2.2mm. The supply voltage is 3.3 V, and our target voltage is 0.6V. Table 4 shows the experimental results of the proposed asynchronous 8051 microprocessor. The experimental results show that the proposed NCL 8051 reduces power consumption by 40% compared with the synchronous 8051. Therefore, it is expected that the conventional synchronous 8051 can be replaced to the proposed NCL 8051 for ultra-low power reliable systems.

EXPERIMENTAL RESULTS

This paper proposes a low power asynchronous 8051 microprocessor using a NCL pipeline structure. The synchronous 8051 microprocessor has been converted into NCL based 8051 microprocessor. The simulation results show that the proposed NCL 8051 reduces power consumption by 40% compared with the synchronous 8051. Based on the experimental results, the proposed NCL 8051 microprocessor will be used in low power required IoT/IoE or biomedical applications.

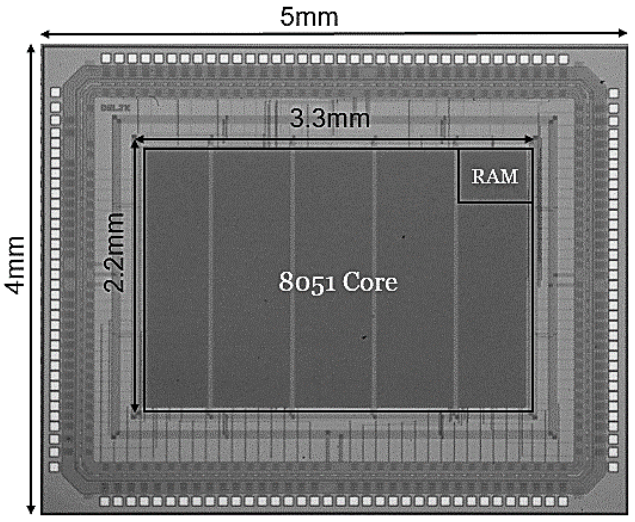

Figure 10: Die photo of the proposed 8051 MCU

Table 4: Experimental results of the proposed 8051.

Core	Area(um^2)	Speed(MHz)
Proposed 8051	14,438.14	10MHz
	Power(W) (Reduction Rate %)	
	Net Switching Power	7.75E-04(8.52%)
	Cell Internal Power	8.30E-03(91.28%)
	Cell Leakage Power	1.77E-05(0.19%)
	Total Power	9.09E-03 (40%)

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