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Implementation of Fusion Technique with Modified Booth Recoder

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Abstract –

Complex Arithmetic operations were carried out in the applications of DSP. The speed of Addition and multiplication has to be increased. A new concept of Adder Multiplier is implemented by using Sum to Modified Booth algorithm bits were generated in its Modified Booth form. The generated partial products were reduced by using Wallace Tree multiplier. Without degrading the performance the power consumption is reduced by using compressor. The 4:2 compressors is chosen which reduces the partial product 4 to 2.The parallel multiplier with the compressor increases the speed, decreases delay thereby reducing power consumption. The output of compressor is given to CLA adder to obtain the final result.

Keywords: Fused Add Multiply (FAM), Sum to Modified Booth (S-MB), Carry Save Adder (CSA)

INTRODUCTION

The emerging modern technology in VLSI integrates millions of transistors on a single silicon semiconductor microchip. CMOS technology is due to its scaling properties the steady state decrease in size allowing for more and more complex systems on a single chip, working at higher clock frequencies. The complexity of today's ICs, is over 100 million transistors is a great challenge. The circuit designers and electronic design automation (EDA) tools concentrate on maximizing circuit performance and minimizing circuit area. The increasing speed and complexity of today's designs implies a significant increase in the power consumption of Very-Large-Scale Integration (VLSI) chips. Different design techniques were developed to reduce power. Now a day's low power VLSI design is attracting all the electronic devices, since power become a major criterion in designing. Today almost all the electronic devices are being used in battery backup for portability and comfort. Reducing the total power consumption in such systems is important, since it is desirable to maximize the run time with minimum requirements on size, battery life and weight allocated to batteries. Parallelism and pipelining in system architecture can reduce power significant. Clock disabling, power-down of selected logic blocks, adiabatic computing, software redesign to lower power dissipation are the other techniques commonly used for low power design. This low power consumption will also helps in reduction of heat dissipation in such electronic devices resulting in wide and long use. The main applications of DSP are audio signal processing, audio compression, digital image processing, video compression, speech processing, speech recognition, and digital communications and so on. Multipliers, Adders are widely used in digital signal processing applications. High speed addition and multiplication is preferred in DSP applications. The speed of adder is delayed, due to the propagation of carry. This has been eliminated by using CLA, CSA adder. Here we developed CSA adder in order to reduce delay and to enhance fast operation. Speed of multiplier is based on reduction of partial product reduction that is achieved with the help of parallel multiplier. Here we chosen Wallace CSA adder tree due to its parallel architecture where the power consumption got reduced. Without degrading the other performance by using compressor the partial product generated is reduced by reducing the power consumption. Here 4:2 compressors are chosen to reduce the partial product into two. The accuracy is main advantage of DSP applications, it relies on the power consumption.

PROPOSED SYSTEM

FUSION OF ADDER AND MULTIPLIER

Adder and Multiplier operator is based on the fusion of adder and the Modified Booth Encoding [1] into a single block by recoding the sum Y=A+B to its MB. So that area has reduced. The MB bit is multiplied with Y. Both X and Y consists of n=2k bits

$$PP_{j=X.}\ y_j^{MB} = \bar{p}_{j,n}2^n + \sum_{i=0}^{n-1} p_{j,i}.2^i \qquad (1)$$

The recoding of the sum of two numbers in its MB form leads to a more efficient implementation of the fused Add-Multiply (FAM) unit [1]. The Sum- Modified Booth algorithm is simple and it can be easily modified in order to apply in signed or unsigned numbers, which consist of odd or even number of bits. Sum-Modified Booth algorithm [2] uses unsigned and signed-bit Full Adders and Half Adders. It obtains an improvement in both area and power consumption. The fused Add-Multiply (FAM) uses only one adder at the end. As a result, area savings is achieved and the critical path delay is reduced .Multiplication involves two basic operations (i) Partial Product Generation (ii) Accumulation. There is two ways to speed up the process either by reducing the partial product or by accelerating the accumulation. Hence forth Modified Booth bit is represented using radix-4[6] rather than radix-2 as it is more efficient.

S-MB RECODING TECHNIQUES

By using signed HAs and FAs three alternative schemes of the *S-MB* recoding technique were developed [3]. The three schemes can be applied in either signed or unsigned numbers which consist of odd or even number of bits. A and B inputs were in 2's complement form and consist of 2k bits in case of even or 2k+1 in case of odd. The three S-MB recoding scheme are:

- ❖ S-MB1 Recoding Scheme
- ❖ S-MB2 Recoding Scheme
- ❖ S-MB3 Recoding Scheme

These S-MB1, S-MB2, S-MB3 Recoding Techniques are implemented by Radix-8 recoding Techniques.

PARTIAL PRODUCT GENERATOR

A product formed by multiplying the multiple and by one digit of the multiplier when the multiplier has more than one digit. Partial products are used as intermediate steps in calculating large products. Partial product generator is designed to produce the product by multiplying the multiple and M by 0, 1, -1,2,- 2,-3,-4, 3, 4. For product generator, multiply by zero means the multiple and is multiplied by "0". Multiply by "1" means the product still remains the same as the multiple and value. Multiply by "-1" means the product is the two's complement form of the number. Multiply by "-2" is to shift left one bit the two's complement of the multiplicand value and multiply by "2" means just shift left the multiple and by one place. . Multiply by "-4" is to shift left two bit the two's complement of the multiple and value and multiply by "2" means just shift left the multiple and by two place.

PARTIAL PRODUCT REDUCTION

The number of partial product steps is reduced by using Wallace tree Multiplier. Wallace tree along with Booth Algorithm reduces the partial products [4]. The Wallace tree construction method is usually used to add the partial products in a tree-like fashion in order to produce two rows of partial products that can be added in the last stage. The Wallace tree [5] is fast since the critical path delay is proportional to the logarithm of the number of bits in the multiplier. The prominent method considers all the bits in each column at a time and compresses them into two bits (a sum and a carry). For compress them into two bits many type of compressor are used such as 4:2 compressor, 3:2 compressor, 5:3 compressor.

It adds n = 8 partial products $m^{(0)}$, $m^{(1)}$, . . . , $m^{(7)}$. Each line represents a number with the number of bits indicated. The left output of each carry-save adder represents the sum bits, and the right output represents the carry bits.

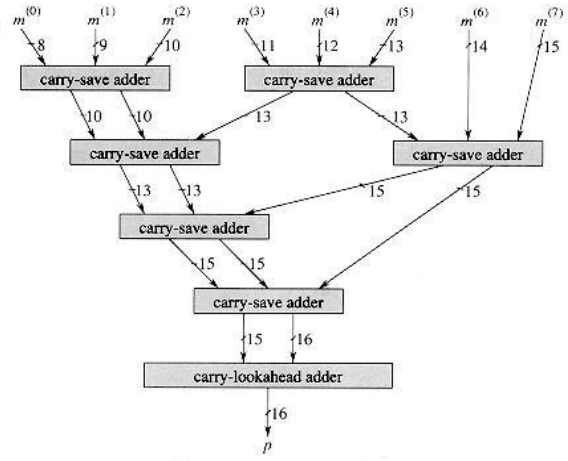

Figure.1. Wallace Tree Diagram

COMPRESSOR

Speed of the multiplier can be increased by reducing the generated partial products. Many attempts have been made to reduce the number of partial products generated in a multiplication process one of them is Wallace tree multiplier. Wallace Tree CSA structures have been used to sum the partial products in reduced time. Speed of the Wallace tree multiplier can be improved by using compressor techniques. Here the Wallace tree is constructed by using traditional method and with the help of compressor 4:2 compressor technique. Therefore, minimizing the number of half adders used in a multiplier reduction will reduce the complexity.

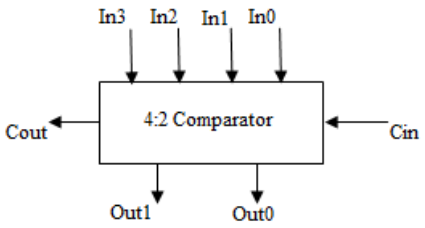

Figure.2. Block Diagram of 4:2 Compressor

CARRY LOOK AHEAD ADDERS

To reduce the computation time, there are faster ways to add two binary numbers by using carry look ahead adders. They work by creating two signals P and G known to be Carry Propagator and Carry Generator [8]**.** The carry propagator is propagates to the next level where as the carry generator is used to generate the output carry, regarding the input carry [9][10].

PERFORMANCE EVALUATION

Analysis made in terms of area, power consumption among three recoding schemes for existing and proposed system. From the following table we observe the difference in area

reduction and power consumption for the three recoding schemes with and without Wallace tree compressor.

Table 1. Comparison of Performance Analysis for Signed Input Bits

Module	Type of function	Existing System		Proposed System	
		Power Consumption	Total number of gates used	Power Consumption	Total number of gates used
FAM1	EVEN	63mW	2434	51mW	1667
	ODD	61mW	2145	50mW	1565
FAM2	EVEN	63mW	2434	50mW	1673
	ODD	62mW	2139	50mW	1565
FAM3	EVEN	63mW	2443	51mW	1673
	ODD	61mW	2190	50mW	1625

Table 2. Comparison of Performance Analysis for Unsigned Input Bits

Module	Type of function	Existing System		Proposed System	
		Power Consumption	Total number of gates used	Power Consumption	Total number of gates used
FAM1	EVEN	163mW	2434	151mW	1131
	ODD	161mW	2145	136mW	1038
FAM2	EVEN	163mW	2434	139mW	1131
	ODD	162mW	2139	110mW	1038
FAM3	EVEN	163mW	2443	117mW	1131
	ODD	161mW	2190	117mW	1038

SIMULATION RESULTS

The three recoding schemes S-MB1, S-MB2, S-MB3 were designed and each of them is used in Fused Add Multiply (FAM) operator. The above concept is implemented using structural VHDL for both even and odd bit width of inputs.

The output of sum to modified booth is given to the Wallace CSA tree and fast CLA. For each timing constraint, the output is simulated using Modelsim m for the same set of pairs of input numbers in 2's complement representation.

The power consumption is calculated for the compressed design and it is compared with the existing one.

Thus we shall conclude that the power consumption and area got reduced by using Wallace Compressor by using it in my design

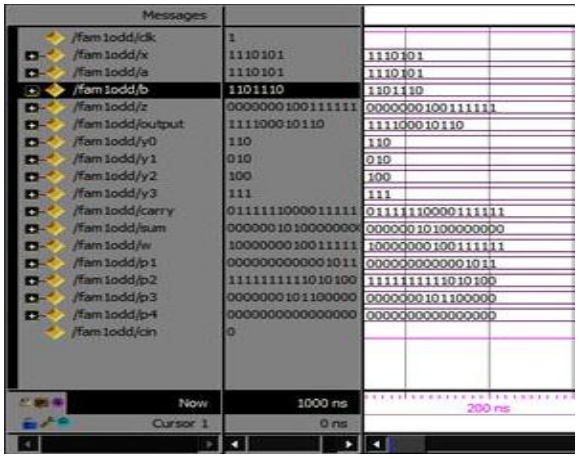

Figure.3. Fused Add multiply for ODD Bit

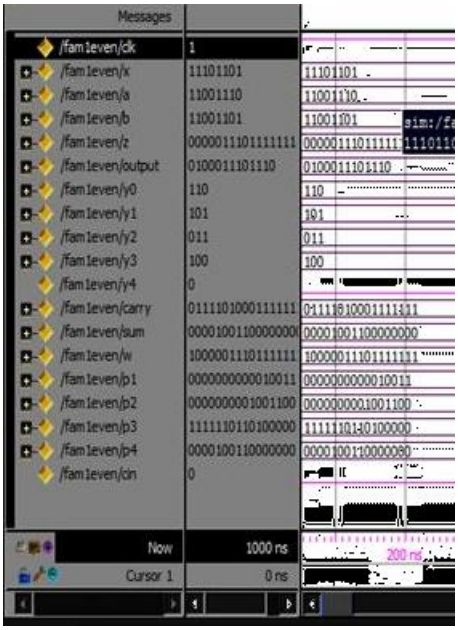

Figure.4. Fused add multiply for EVEN Bit

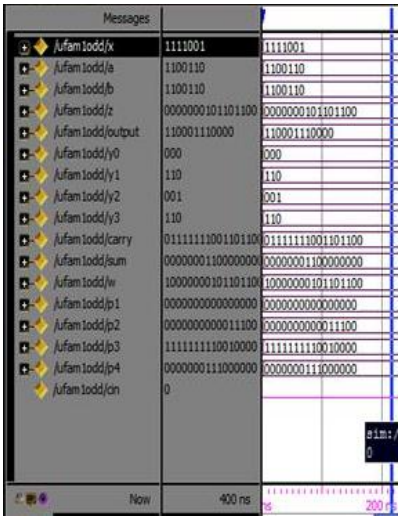

Figure. 5. Unsigned Fused add multiply for ODD Bit

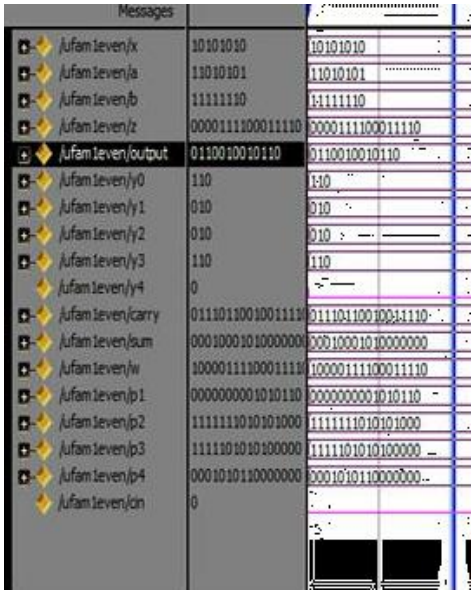

Figure. 6. Unsigned Fused add multiply for EVEN Bit

CONCLUSION

By using Fused Add Multiply the number of adders used in the circuit got reduced, which in turn reduces the area, power consumption and delay .By using Modified Booth Recoding the partial product generated was reduced into half. The generated partial products were added using Wallace Carry Save Adder. The Modified Wallace Tree with Compressor reduces the number of adders used in the circuits which in turn reduces the circuit complexity. As the compressor order is increases the time delay reduces respectively. Hence for small delay requirement Wallace Tree Multiplier using Compressor is chosen.

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