

# Design of BCD Compressors Using Vinculum Code for Efficient Multiplication

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## Abstract

Compressors play a very important role in multipliers for adding partial products. Decimal Computations has grown interest in recent years due to the availability in its hardware architectures.

In literature binary compressors are available but decimal compressors are not that much exposed. This paper gives a basic principle of 3:2 decimal VBCD compressors with three operands of 4bit each. It uses a binary full adder for adding bits and simple correction circuit. This structure can be used to add partial products in multiplier. This paper presents from a basic 3:2 compressor to 8:2 compressor. The simulation have been carried out in Cadence Digital Encounter TSMC 180nm technology and were compared with decimal compressors.

**Keywords:** Decimal Compressors, Full Adder, performance

## INTRODUCTION

Multiplication is very basic operation for any computing system[1]. Even though most of the systems are in binary there are few applications which uses only decimal number system which cannot be changed forever. So to meet these applications we require processors which work on decimal number system. These processors require an ALU which performs all arithmetic operations on decimal number system.

Many architectures uses converters from decimal to binary and vice versa for their computations where lot of time takes for computation. Lot of literature exists on decimal multipliers with code converters, using various number representations like 5211, 4221, excess3 code etc for implementation of multipliers.

These involves variety ways of adding partial products like array multipliers, carry save adders and carry look adders for better efficiency. Although tree multipliers exist for faster multipliers they are irregular in structures which affect its performance. This lead to the investigation of regular structures and one solution is to employ special adder, called a compressor that enables the reduction of partial product tree in more regular fashion[5]. A simple full adder in binary is equivalent to 3:2 compressor which acts as basic building block for other compressors. It has three inputs (a, b, c<sub>in</sub>) and

two outputs sum & carry. 3:2 Decimal compressor consists of three operands of 4bits each (x,y,z) with two outputs sum & carry. Intermediate carries will be forwarded to the next stage. 4:2 compressors use two 3:2 compressors and so on.

The most common decimal encoding is 4 bit BCD which represents decimal codes 0 to 9. But with 4 bits we can represent 16 combinations out of which only 10 different combinations are used. The reset of the combinations are unused and those combinations must be eliminated. So Efficient addition of decimal numbers is an interesting topic because these are further used in multipliers. Very little literature exists on this where author uses two methods to add numbers. These are Decimal carry save addition [4] and signed digit addition. But in paper [4] author described only carry save addition.

## VINCULUM NUMBER REPRESENTATION

Vinculum is a method of number representation where bigger digits like 6,7,8,9 are represented using smaller numbers 4, 3, 2, 1 as follows: 6 is represented as  $1\bar{4}$  (meaning 10-4). Similarly 7 is represented as  $1\bar{3}$ , (10-3), 8 is represented as  $1\bar{2}$  and 9 is represented as  $1\bar{1}$ . Hence 6,7,8,9 are not in the set of vinculum numbers. They are alternatively represented using the vinculum set which constitutes the following numbers as its elements {0, 1, 2, 3, 4, 5,  $\bar{4}$ ,  $\bar{3}$ ,  $\bar{2}$ ,  $\bar{1}$ }. Each Vinculum digit can be represented in binary as {0000, 0001, 0010, 0011, 0100, 0101, 1100, 1101, 1110, 1111} [9].

## EXISTING METHODS

Very small work had done on decimal compressors. In [5] author designed 3:2, 4:2, 8:2 and 16:2 compressors based on various coding techniques. In this paper author used 4221 and 5211 codes and recoding from one to another had done. The resultant expression was  $S+2H$  where S is the final sum and H is the recoded number and 2 is the weightage. In another paper [8] author designed 4:2 and 5:2 compressors based on unconventional recoding scheme for implementation. The codes that includes 4221, 5211, 3321 etc where all the combinations are suitable for arithmetic operations. In this author used 4221 similar to paper[5]

**DECIMAL 3:2 VBCD COMPRESSOR**

A decimal compressor is a circuit which takes three input operands and produces two outputs in terms of Sum and Carry. Algorithm is explained as below

Algorithm for Compressor.

step 1: Read input operands as x, y, z of 4 bit each in VBCD form  
 step 2: Set output digits as Sum and Carry bits  
 step 3: Add bit wise operands using Full Adders and check for Sum and Carry bits  
 case 1: If sum < 5 or if sum < -4 and carry = 1 discard carry bit and take Final sum = sum  
 Case 2: If sum > 5 and carry = 0, Add + 6 to the sum and set carry = 1  
 Case 3: If sum > 5 and carry = 1 add - 6 to the sum and set carry = -1

Operands	Vinculum Number	Binary Value
A	2	0 0 1 0
B	1'	1 1 1 1
C	3	0 0 1 1
intermed iate sum		1 1 1 0
Carry	0	0 1 1
Final Sum	4	0 1 0 0
carry		0

Figure 1. Decimal 3:2 compressor

In the above example each bit of the operand is passed through full adder which results in intermediate sum and carry bits. It is added with carry bits to get final sum. If final sum is greater than 5 and carry bit '0' add 6 to it and take carry bit 1.

The architecture of the compressor has been implemented through binary full adders, 2x1 multiplexer and adder/subtractor circuit. The architecture has been shown in figure [2]&[3] with four binary full adders to add three decimal digits with addition of +/- 6 as correction factor.

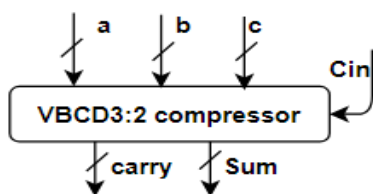


Figure 2. 3:2 VBCD Compressor

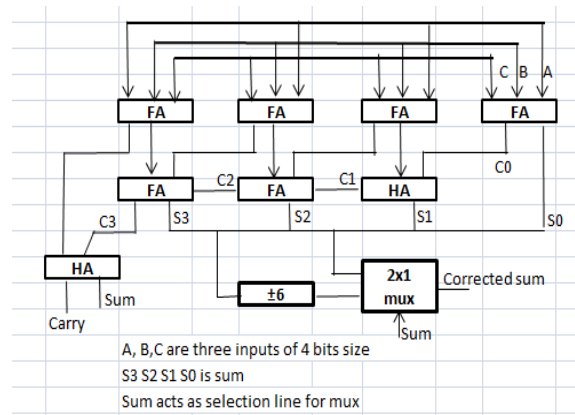


Figure 3. Basic Architecture of 3:2 Compressor

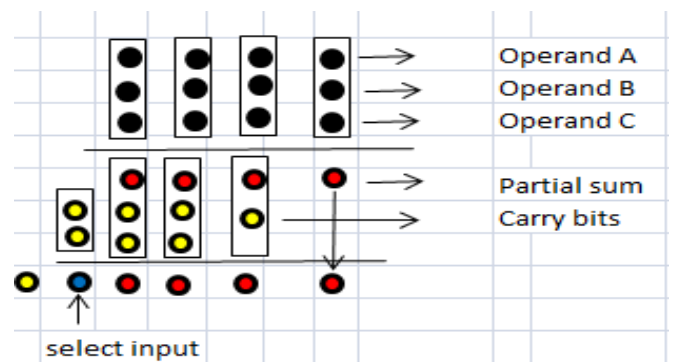


Figure 4. Dot representation of 3:2 compressor

In figure 4 black dots indicates partial products, red dots indicates partial sum and final carry outputs.

**4:2 Compressor:**

4:2 compressor consists of four operands and input carry as its inputs with two outputs Sum and carry along with intermediate carry out to the next stage as shown in the figure [4]. It comprises of two 3:2 compressors where first three operands are given to 3:2 compressor1 and the output sum digit, fourth operand along with carry input is given to 2nd compressor 3:2. The output carry bit of first compressor is passed to next stage. This makes compressor more faster than other adders. The weightage of the carry digit increases as the inputs increases. Same weightage of digits can be taken together for any digit compressor's inputs.

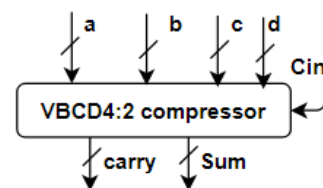


Figure 5. 4:2 VBCD Compressor

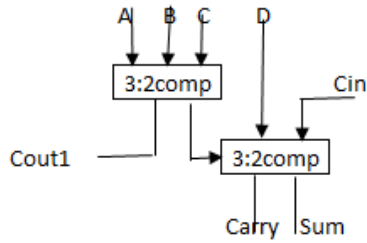


Figure 6. 4:2 compressor using 3:2 compressors

**5:2 Compressor:**

5:2 Compressors consists of five operands (A,B,C,D,E) and input carry with two outputs sum and carry as final inputs. It consists of two intermediate carry outs which follows to the next stage. This can be constructed using two 3:2 compressors as shown in the figure[8].

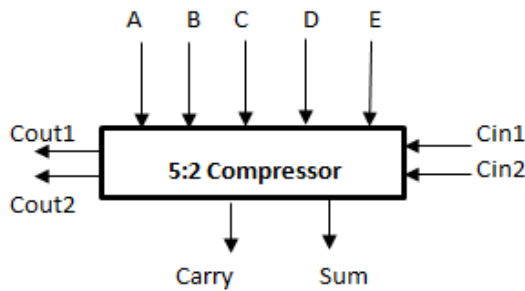


Figure 7. 5:2 VBCD Compressor

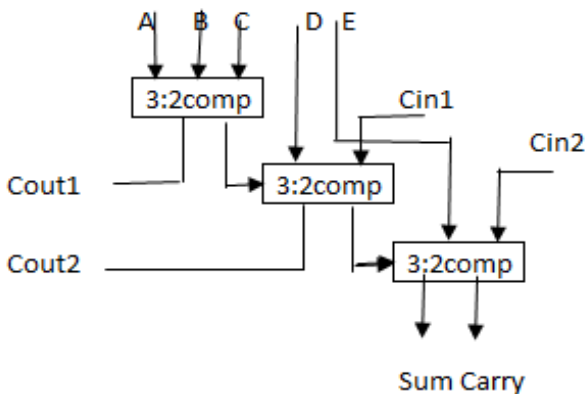


Figure 8. 5:2 Compressor using 3:2 compressors

The main advantage of using the proposed new compressor 4:2 is that the carry out is not dependent on carry in. This allows partial product reduction trees to be built more easily and with regularity. Using this basic architecture we can build any type of compressor.

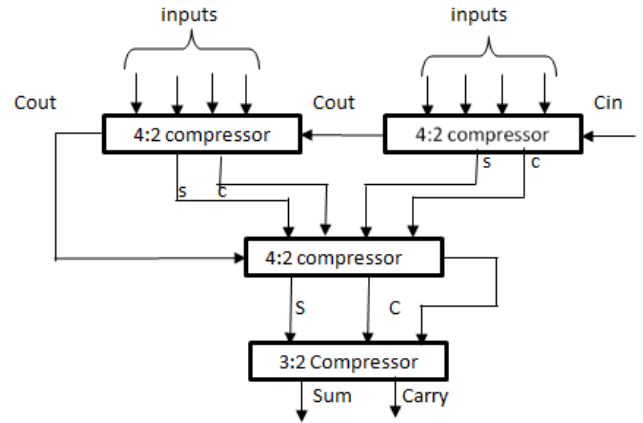


Figure 9. 8:2 Compressor

Figure 9 shows the designing of 8:2 compressor using 4:2 compressors and 3:2 compressor in a systematic manner. Similarly we can implement 16:2 also.

**RESULTS**

The table 1 shows the results for the proposed compressors from 3:2 to 8:2. We can implement the same even for more operands. A Verilog code has been developed for each compressor based on Vinculum digit set [-4,5] and synthesized using Cadence Digital Encounter Tools TSMC 180nm technology. To verify its functionality each one is tested for all possible combination of input test vectors.

Table 1: Results of compressors using Xilinx ISE simulator 14.2i

Sl. No.	Type of Comp	Slice LUT's	IOB's	Delay (ns)
1	3:2	22	18	5.035
2	4:2	33	30	6.091
3	5:2	40	34	6.801
4.	8:2	58	69	7.210

Table 2: Cadence implementation of compressors

Sl. No.	Type of Comp	Parameter	Ref	Proposed
1	8:2	Delay(ns)	3.32	2.89
		Area(µm <sup>2</sup> )	7600	4215
3	16:2	Delay(ns)	4.87	3.91
		Area(µm <sup>2</sup> )	16,917	9370

**CONCLUSION AND FUTURE SCOPE**

In this paper we made an attempt of decimal compressors using Vinculum number system. We implemented using simple binary full adders with a simple correction logic. Performance parameters like Area, Power and Delay are compared with other architectures. For small operand sizes it

does not provide a substantial benefit but as operand size increases it has greater advantage. So this concept was used in Multiplier to add partial products of various lengths.

In future we will use these in adding partial products in multiplier architectures.

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