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Analysis of MOS transistor behavior with Forward and Reverse Body biasing in Subthreshold region

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Abstract

All future vlsi circuits need to operate with ultra low power. Circuits operating with supply voltage as low as threshold voltage of MOS transistors. Subthreshold region offers energy efficient circuits but degrades the performance. Body biasing techniques made a comeback to have high speed and low power circuit operation in subthreshold region. Conventional CMOS itself is energy efficient with decreased performance at low supply voltages. Several body biasing methods exists in literature to improve performance Near/Below V_t supply voltages. In the paper MOS transistor characteristics are analyzed in subthresold region with different body biasing methods with Vdd=0.4v with PMOS and NMOS with 200nm, 400nm width respectively. Simulated using Cadence 45nm technology tool. Proposed new body biasing technique with fixed bias voltage between source and bulk which give better results than existing one.

Index Terms— *Body bias, Forward body bias, Reverse body bias, Fixed bias voltage, Subthreshold region, Body bias voltage generator.*

INTRODUCTION

MOS transistor operates in different regions like super threshold (STV), Near threshold (NTV) and subthreshold based on requirement of the applications. Nowadays subthreshold design is area of interest for many researchers to have portable devices with more functionality and for long battery life. When operating voltage becomes transistor ON threshold both dynamic and static power get reduced at this point both powers are almost comparable.[1][8]

Body biasing techniques resolve the problem of increased leakage currents and decreased speed of subthreshold circuits. Body biasing is a old method by applying to circuits which operates with low voltage gives moderate performance. Body biasing adjusts threshold voltage by applying voltage between source and substrate of each MOS transistor [2].

MOS transistor threshold voltage is related with source to bulk voltage as in the below mathematical expression:

$$V_{th}=V_{to}+\gamma(\sqrt{\varphi s + Vsb} - \sqrt{\varphi s})\text{------}(1)$$

Where V_{to} is threshold voltage with zero body bias, γ is body effect factor, φs surface potential and Vsb voltage between source and substrate.

By decreasing Vsb threshold voltage of the device decreases to speed up the operation and increasing Vsb increases threshold voltage to reduced the leakage currents of OFF devices.

In static CMOS circuits source to substrate voltage is zero because PMOS transistor source and substrate are connected to Vdd and NMOS transistor substrate are connected to ground potential. Source to bulk voltages can have non zero values by different body biasing methods. DTMOS, Swapped, VTCMOS, Forward body bias (FBB) and Reverse body bias (RBB) are some methods to control threshold voltage.

DTMOS varies threshold voltage dynamically with input voltage by connecting each transistor substrate to gate. When the device is ON threshold voltage decreases increases the drive current to speed up the operation. CMOS and DTMOS have similar transistor operation during OFF mode.[3]

Swapped body biasing substrate of PMOS is connected ground potential and substrate of NMOS is connected to supply rail. This increases both drive current and leakage of ON, OFF transistors respectively [3].

A fixed bias voltage between source and substrate is used to decrease and increase device threshold voltage. ON transistor threshold voltage is decreased by applying FBB to reduce short channel effects at lower voltages. OFF transistor threshold voltage is increased by applying RBB to minimize leakage currents [4].

CMOS inverter is designed with different body biasing methods to verify all these effects in each transistor. Tabulated results in section V.

EFFECT OF BODY BIASING IN SUBTHRESHOLD REGION

Body biasing for scaled CMOS devices reduces short channel effects and process variations. Subthreshold, BTBT and gate leakage are mainly affected in all leakage currents. Body

biasing either increases or decreases the threshold voltage. Subthreshold leakage current and threshold voltage are exponentially related in weak inversion region [5].

NMOS and PMOS subthreshold currents are related with below expressions [6]:

$$I_{DS}=\beta_N e^{\frac{V_{GS,N}-V_{TH,N}}{n_N V_T}}\left(1-e^{\frac{V_{DS,N}}{V_T}}\right) \text{---------------(2)}$$

Where $\beta_N=\mu_N C_{OX}\left(\frac{Wn}{Ln}\right) V_T^2(n_N-1)$

$$I_{SD}=\beta_P e^{\frac{V_{GS,P}-V_{TH,P}}{n_P V_T}}\left(1-e^{\frac{V_{DS,P}}{V_T}}\right) \text{---------------(3)}$$

Where $\beta_P=\mu_P C_{OX}\left(\frac{Wp}{Lp}\right) V_T^2(n_P-1)$

where βN (βP) is the subthreshold current factor for the nMOS (pMOS) transistor, VGS,N (VSG,P) is the gate-to-source (source-to-gate) voltage for the nMOS (pMOS) transistor, VTH,N (VTH,P) is the threshold voltage of the nMOS (pMOS) transistor , VDS,N (VSD,P) is the drain-to-source (source-to-drain) voltage of the nMOS (pMOS) transistor , μN (μP) is the electron (hole) mobility, C_{OX} is the oxide capacitance per unit area, W is the channel width, L is the channel length of nMOS and pMOS, VT = kT/q (with k Boltzmann constant, T absolute temperature and q elementary charge) is the thermal voltage and nN (nP) is the subthreshold slope factor for the nMOS (pMOS) transistor [6].

Band- to-Band Tunneling (BTBT) leakage current is also effected by bias voltage. Reverse body biasing rapidly increase tunneling current where as forward bias decreases slowly [5].

The reduction of gate oxide in scaled devices gives rises to gate leakage current. This is due to three main leakages i.e. gate to drain, gate to substrate and gate to source leakage. It is less sensitive to bias voltage than tunneling current [5].

CMOS INVERTER IMPLEMENTATION WITH FBB AND RBB IN SUBTHRESHOLD REGION

CMOS Inverter in Fig 1 and 2 is designed in region 3 using cadence virtuoso schematic composer to analyze operation in sub threshold region. Characteristics of MOS transistor observed for both low and high inputs individually.

For low input PMOS is FBB and NMOS is RBB to overcome performance degradation at ultra low supply voltages.

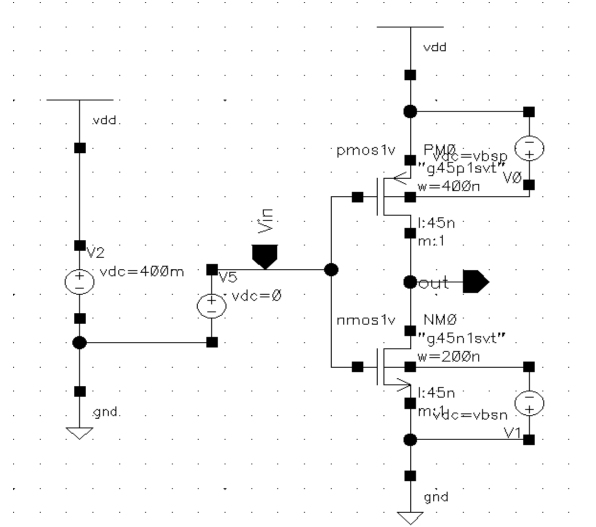

Figure 1. CMOS Inverter schematic with low input voltage with respective Body biasing of transistors

For high input PMOS is RBB and NMOS is FBB under DC analysis operating characteristics are noted.

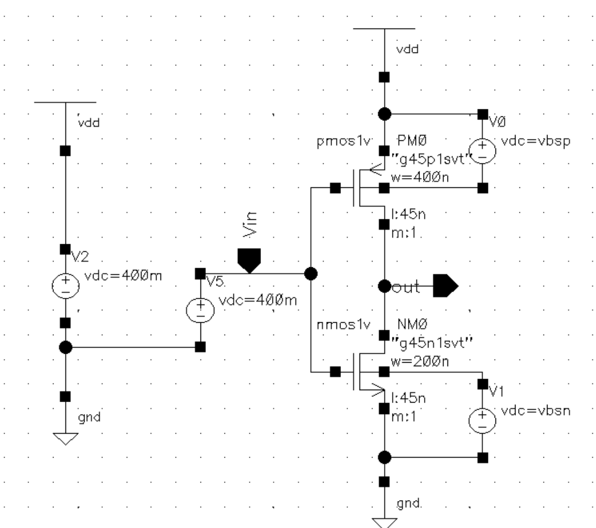

Figure 2. CMOS Inverter schematic with high input voltage with respective Body biasing of transistors

BODY BIAS GENERATOR CIRCUITS

Circuits designed in subthreshold region with body biasing consists two sub circuits: Logic circuit which implements the required functionality and Body bias Generator (BBG) circuit to provide bias voltage to each transistor. There are multiple ways to do body biasing.

A bias control circuitry based on simple pass transistors action is shown in fig 3. Below BBG circuit reduces the threshold voltage of ON transistor to speed up the operation and OFF transistor threshold voltage increases to minimize static power consumption.

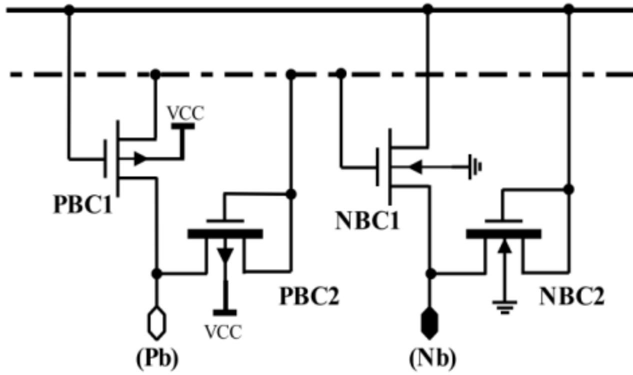

Figure 3. The body bias control circuit

Input voltage for MOS transistor decides whether respective transistor threshold voltage to be increased or decreased. For low level input threshold voltage should be decreased for PMOS and increase for NMOS. Similarly for high input it is vice versa. Circuit has one primary input other bias control voltage. PBC1 and PBC2 two transistors apply Vdd-ΔV and Vdd+ΔV to PMOS transistor substrate. NBC1 and NBC2 two transistors apply Vss+ΔV and Vss-ΔV to NMOS transistor bodies based on standby and active mode of operation [7].

One more BBG circuit is shown in below fig 4, it consists two sub circuits one logic circuit other is body bias generator which provides bias voltages to all transistor substrates. Bias circuit is a push-pull amplifier which acts as a voltage follower. When V_{OUT} is Vdd (0V) bias voltage generator supplies high(low) voltages to bodies of all transistors [6].

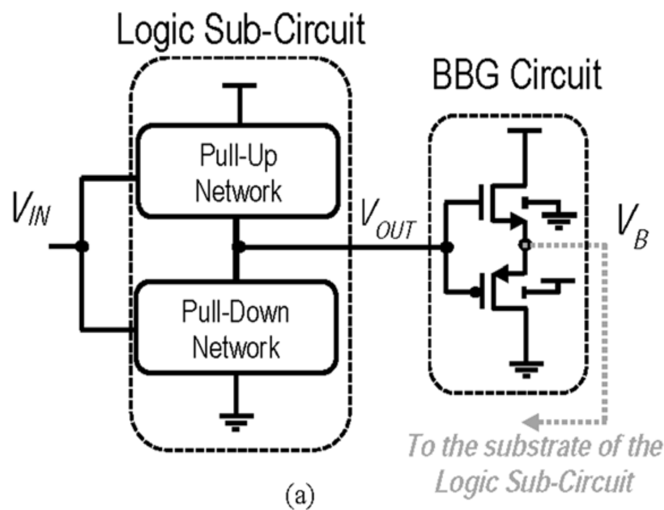

Figure 4. Logic gate with gate-level dynamic body biasing

RESULTS

Table I. Conventional CMOS Inverter characteristics in subthreshold region with low and high inputs

INPUT	MOS Transistor	I_{ds}(A)	Pwr(W)	R_{on}(Ω)	V_{bs}(V)	V_{th}(V)
LOW	PMOS	-3.954p	4.586a	382.6K	0	-566.5m
	NMOS	2.220p	915.1f	180.1G	0	600.1m
HIGH	PMOS	-1.231p	814.0f	324.8G	0	-564.9m
	NMOS	2.928p	4.092a	492.9K	0	618.9m

Table II. CMOS Inverter characteristics in subthreshold region with low and high inputs using DTCMOS body biasing technique

INPUT	MOS Transistor	I_{ds}	Pwr	R_{on}	V_{bs}	V_{th}
LOW	PMOS	-13.58p	7.341p	75.32K	-400m	-495.6m
	NMOS	2.220p	915.1f	180.1G	0	600.1m
HIGH	PMOS	-1.231p	814.0f	324.8G	0	-564.9m
	NMOS	6.286p	2.370p	148.0K	400m	561.7m

By observing results of DTMOS it improves speed of ON transistor and OFF transistors behaves similar to conventional CMOS.

Table III. CMOS Inverter characteristics in subthreshold region with low and high inputs using SWAPPED body biasing technique

INPUT	MOS Transistor	I_{ds}(A)	Pwr(W)	R_{on}(Ω)	V_{bs}(V)	V_{th}(V)
LOW	PMOS	-37.47p	7.341p	75.32K	-400m	-495.6m
	NMOS	26.52p	11.82p	15.08G	400m	537.6m
HIGH	PMOS	-22.29p	12.91p	17.95G	-400m	-494.2m
	NMOS	26.94p	2.370p	148.0K	400m	561.7m

By inspecting results of swapped body bias it increases both ON and OFF transistor power which results into high leakage.

Table IV. CMOS Inverter characteristics in subthreshold region with low input using VTMOS body biasing technique

Fixed bias Voltage	MOS Transistor	I_{ds}(A)	Pwr(W)	R_{on}(Ω)	V_{bs}(V)	V_{th}(V)
0	PMOS	-13.58p	7.541p	75.32K	-400m	-495.6m
	NMOS	2.220p	915.1f	180.1G	0	600.1m
0.1	PMOS	-3.691p	115.2f	114.0K	-300m	-515.2m
	NMOS	1.314p	552.7f	304.3G	-100m	613.7m
0.2	PMOS	-3.005p	1.601f	171.7K	-200m	-533.5m
	NMOS	816.5f	353.6f	489.9G	-200m	626.0m
0.4	PMOS	-2.518p	1.536a	382.6K	0	-566.6m
	NMOS	335.2f	161.1f	1.193T	-400m	649.0m

TABLE V CMOS Inverter characteristics in subthreshold region with High input using VTMOS body biasing technique

Fixed bias Voltage	MOS Transistor	I_{ds}(A)	Pwr(W)	R_{on}(Ω)	V_{bs}(V)	V_{th}(V)
0	PMOS	-1.231p	814.0f	324.8G	0	-565.0m
	NMOS	6.286p	2.370p	148.0K	400m	561.8m
0.1	PMOS	-2.348p	1.260p	170.4G	-100m	-549.0m
	NMOS	145.9p	141.5p	109.1K	500m	545.6m
0.2	PMOS	-4.683p	2.192p	85.30G	-200m	-532.0m
	NMOS	6.626n	8.027n	82.10K	600m	529.4m
0.4	PMOS	-20.19p	10.09p	15.38G	-400m	-494.5m
	NMOS	485.1n	12.63u	184.5K	800m	511.4m

At zero bias voltage VTMOS behave like DTMOS. For low input by increasing bias voltage both transistors power decreases and with high level input increases.

TABLE VI. CMOS Inverter characteristics in subthreshold region with Low level input with PMOS FBB and NMOS RBB

Fixed bias Voltage	MOS Transistor	I_{ds}(A)	Pwr(W)	R_{on}(Ω)	V_{bs}(V)	V_{th}(V)
0	PMOS	-3.954p	4.586a	382.6K	0	-566.5m
	NMOS	2.220p	915.1f	180.1G	0	600.1m
0.1	PMOS	-3.291p	15.79a	256.9K	-100m	-550.5m
	NMOS	1.314p	552.7f	304.3G	-100m	613.7m
0.2	PMOS	-3.005p	1.601f	171.6K	-200m	-533.5m
	NMOS	816.5f	353.5f	489.8G	-200m	626.0m
0.3	PMOS	-3.095p	115.2f	114.0K	-300m	-515.2m
	NMOS	518.3f	234.3f	771.7G	-300m	637.7m
0.4	PMOS	-12.09p	7.341p	75.31K	-400m	-495.6m
	NMOS	335.2f	161.0f	1.193T	-400m	649.0m

TABLE VI. CMOS Inverter characteristics in subthreshold region with High level input with PMOS RBB and NMOS FBB

Fixed bias Voltage	MOS Transistor	I_{ds}(A)	Pwr(W)	R_{on}(Ω)	V_{bs}(V)	V_{th}(V)
0	PMOS	-1.231p	814.0f	324.8G	0	-564.9m
	NMOS	2.928p	4.092a	492.9K	0	618.9m
0.1	PMOS	-671.5f	590.0f	595.6G	100m	-580.0m
	NMOS	2.567p	7.650a	366.5K	100m	605.7m
0.2	PMOS	-378.7f	472.9f	1.056T	200m	-594.3m
	NMOS	2.474p	520.7a	271.7K	200m	591.8m
0.3	PMOS	-219.9f	409.4f	1.819T	300m	-607.8m
	NMOS	2.575p	37.21f	200.8K	300m	577.2m
0.4	PMOS	-131.0f	373.8f	3.053T	400m	-620.8m
	NMOS	5.586p	2.370p	148.0K	400m	561.8m

At zero bias voltage novel bias circuit functions similar to conventional static CMOS. For both inputs by increasing bias voltage moderately increases Active transistor speed and decreases leakage currents of standby device .

CONCLUSION

In this paper CMOS inverter is designed to operate in subthreshold region with different body biasing techniques to improve the working device performance and to decrease leakage currents of OFF transistors further more than the conventional CMOS. Proposed FBB and RBB methods give better power results compared to VTCMOS in subthreshold region with different fixed bias voltages. Discussed how to generate bias voltages using different body bias Generator (BBG) circuits. Body biasing techniques greatly reduces leakage currents for scaled devices at low voltages. CMOS circuits are highlyensitive to process and temperature variations. So we need to adopt a technique more robust against process and temperature variations.

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