

# Design of Common Source Low Noise Amplifier with Inductive Source Degeneration in Deep Submicron CMOS Processes

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## Abstract:

In this paper, inductively degenerated common source Low Noise Amplifier (LNA) is designed using basic equations to meet the Radio Frequency (RF) range of 2.45 GHz - 2.85 GHz. The LNA circuit parameters and transistor geometries are identified from the basic equations by considering 180 nm, 130 nm and 90 nm Predictive Technology Models (PTM) models. The schematic capture of the degenerated LNA is carried out in Advanced Design Software (ADS) environment by tuning the library files and LNA parameters. From the simulation results the designed LNA has a maximum gain of 17.156 dB and minimum noise figure of 0.189 dB with a gate width of 200  $\mu\text{m}$ . The designed LNA has a noise figure less than 2.5 dB and gain greater than 10 dB and hence suitable for Bluetooth applications.

**Keywords:** Low Noise Amplifier, noise figure, RF receiver, wireless networks, Bluetooth, ADS, CMOS, Inductive source degeneration.

## INTRODUCTION

A Low-Noise Amplifier (LNA) is the critical component in the analog front end of a Radio Frequency (RF) receiver [1]. The LNA is responsible for providing sufficient amplification of weak input signals while minimizing the amount of added noise and distortion. As a result, the characteristics of the LNA set the upper limit on the performance of the overall receiver communication system. The optimized design of the LNA is a complex task involving tradeoffs that must be made among several competing parameters including noise figure, gain, linearity, and impedance matching[2]. The design of CMOS LNA should make best trade-off between noise figure, gain, power consumption and chip area. The lumped components in the design of electronic devices are frequency dependent, whose reactance values will change as the frequency increases or decreases [3].

Low-noise amplifiers are designed to minimize the additional noise in RF receiver which affects the performance of RF circuit components. Five characteristics of LNA design are under the designer's control and directly affect receiver sensitivity: noise figure, gain, bandwidth, linearity, and dynamic range. Controlling these characteristics, however, requires an understanding of the active device, impedance

matching, details of fabrication and assembly to create an amplifier that achieves optimal performance with the fewest trade-offs. Designers minimize the additional noise by considering tradeoffs that include impedance matching, choosing the amplifier technology and selecting low-noise biasing conditions. There are several Low Noise Amplifier topologies such as the distributed amplifier topology, common gate, common source, cascade and current reuse topology are the important topologies [4]. Out of these the most frequently used topology for LNA design is the common source topology. With inductive source degeneration, LNA has typically been the best choice for narrowband applications due to its low Noise Figure (NF), high gain and low power consumption with good performance. Both the input matching and the resonator load are capable of handling bandwidths (BW) of several hundred MHz. The input matching circuit consisting of the source inductors and the gate to source capacitance,  $C_{gs}$ , resonates at a single frequency[5, 6]. The application of Bluetooth system is not satisfactory as the system uses low power signals in ISM (Industrial devices, Scientific and Medical) band [7, 8]. Designing a Low Noise Amplifier for Bluetooth applications and its simulation setup in ADS are presented in 'LNA Design Methodology' section and in 'Experimental Setup and Validation' section. Simulation results are reported in 'Gain and Noise Figure Simulation Results Discussion' section. 'Conclusion' section provides the conclusion.

## LNA DESIGN METHODOLOGY

The common source LNA with inductive source degeneration is shown in Figure 1. The 50 Ohm resistor  $R_s$  is connected across the input terminal of LNA and hence providing the input matching. The bandwidth of the amplifier is determined by the input capacitance,  $C_{gs}$  of the transistor  $M_1$  and is very large. The inductance  $L_g$  at the gate of NMOS removes the gate to source capacitance of  $M_1$  at the resonant frequency and hence making the impedance at the input of NMOS to be real i.e., only input resistance  $R_{in}$ . A step by step algorithmic design methodology has been developed for common source LNA with inductive source degeneration in the following section [9].

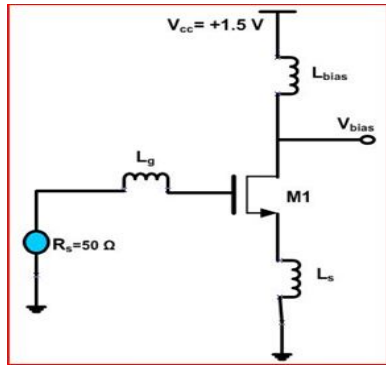


Figure 1. Common Source CMOS LNA

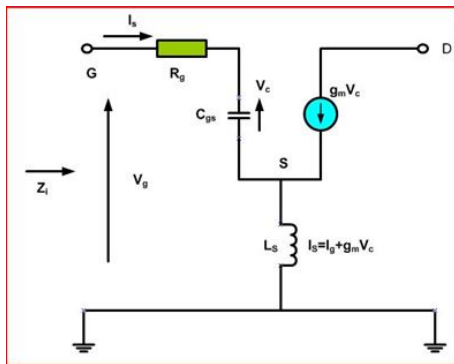


Figure 2. Small signal model of CS LNA

### a) The Design Methodology

The small signal model of transistor with source degeneration is as shown in Figure 2. The small signal model input impedance  $Z_{in}$  of the circuit is given by equation (1)

$$Z_{in} = \frac{V_g}{I_g} = \frac{(I_g R_g + V_c + j\omega L_s L_s)}{I_g} \quad (1)$$

The voltage across the capacitor,  $V_c$  is expressed in the ratio of  $I_g$  and  $C_{gs}$  [10]:

$$V_c = \frac{I_g}{s C_{gs}}; I_s = I_g + g_m V_c; g_m = \mu_n C_{ox} \frac{W}{L_{min}} V_{eff} \quad (2)$$

Substituting equation (2) in equation (1) and the simplified equation is given by equation (3).

$$R_{in} = R_g + R_a + j[X_{L_s} - X_{C_{gs}}] \text{ where } R_a = \frac{L_s g_m}{C_{gs}} \quad (3)$$

With  $R_g = 0$  and impedance without feedback is

$$R_{in} = R_g - jX_{C_{gs}} \rightarrow R_{in} = -jX_{C_{gs}}$$

By adding the series feedback the term  $R_a + jX_{L_s}$  is added to the original input impedance  $Z_{in}$ .

Another inductor  $L_s$  is added in series with  $L_g$  to resonate with capacitor  $C_{gs}$  [11, 12]:

$$R_{in} = \frac{L_s g_m}{C_{gs}} = 50 \Omega \text{ with } j\left(\omega L_s - \frac{1}{\omega C_{gs}}\right) = 0$$

### b) Design Example

The narrow band LNA circuit shown in Figure 1 and the corresponding specifications of LNA is given in Table 1. Considering the above parameters the transistor geometry and LNA parameters are computed using Predictive Technology Model 180 nm.

Table 1. Narrow band LNA specifications

Parameters	Frequency (GHz)	Noise Figure (dB)	Gain (dB)	Source/Load Impedance(Ohms)
Specifications	2.45 to 2.85	< 2.5	> 10	50

The value of degeneration inductor  $L_s$  depends on the maximum size of inductance allowed by the process technology, as  $L_s = 0.5 \text{ nH}$  the cutoff frequency  $\omega_T$  is computed as in equation (4)

$$\omega_T = \frac{g_m}{C_{gs}} = \frac{R_s}{L_s} = 1 \times 10^{11} \text{ rad/sec} (\sim 16 \text{ GHz}) \quad (4)$$

The optimal quality factor  $Q_L$  of inductor with  $\rho = 0.162$  is given by equation (5), where  $\rho = \frac{\delta \alpha^2}{5 \gamma}$ , the parameters for  $\rho$  are dependent on the technology but typically  $\gamma$  is set between 2 - 3 (normally 2),  $\delta$  is set to 2 - 3 times the value of  $\gamma$  (normally 4),  $\alpha$  is assumed to be 0.8 - 1 (taken to be 0.9)

$$Q_L = \sqrt{1 + \frac{1}{\rho}} = 2.67 \quad (5)$$

The value of gate inductor  $L_g$  is given by equation (6)

$$L_g = \frac{Q_L R_s}{\omega_o} - L_s = 7.52 \text{ nH} \quad (6)$$

$$W_o = \frac{1}{\sqrt{(L_g + L_s) C_{gs}}}$$

Where  $W_o$  is the resonance frequency [13].

### Design of LNA for Predictive Technology Model (PTM) 180nm

The width ( $W$ ) of the transistor is given by equation (7),

$$W = \frac{3 C_{gs}}{2 C_{ox} L_{min}} = 434 \mu\text{m} \quad (7)$$

Where  $C_{gs}$  is the gate to source capacitance,  $C_{ox}$  is the oxide capacitance and  $L_{min}$  is the minimum channel length which is 180 nm.

The effective transconductance  $g_m$  of CS LNA is given by equation (8),

$$g_m = \omega_T \cdot C_{gs} = 0.045 \text{ A/V} \quad (8)$$

$\omega_T = 2\pi f_T$ , where  $f_T$  is the unity gain frequency of the MOS transistor.

The effective voltage applied to MOSFET is computed in equation (9),

$$V_{eff} = V_{gs} - V_t = \frac{g_m \cdot L_{min}}{\mu_n C_{ox} W} = 61.78 \text{ mV} \quad (9)$$

The gate to source voltage  $V_{gs}$  is varied from 0.5 V to 1 V. Where  $\mu_n$  is the mobility of charge carriers and  $w$  is the width of transistor.

The bias current  $I_D$  is calculated by substituting the results of equation (8) and equation (9) as in equation (10),

$$I_D = \frac{1}{2} \cdot g_m \cdot V_{eff} = 1.39 \text{ mA} \quad (10)$$

The Estimated Optimum Noise Figure is given in equation (11) with the centre frequency  $\omega_o$

$$NF_{opt} = 1 + \frac{2\gamma}{\alpha} \left( \frac{\omega_o}{\omega_T} \right) \sqrt{p(|c| + \sqrt{p} + \sqrt{1+p})} = 2.12 = 20 \log(2.12) = 3.26 \text{ dB} \quad (11)$$

### c) Design Calculations

The LNA is designed and circuit parameters have been computed by considering PTM 180 nm, PTM 130 nm and PTM 90 nm models. The circuit parameters of the proposed LNA are summarized in Table2. The Process-dependent parameters for 90 nm, 130nm and 180 nm technology nodes were derived from the model files provided by PTM[14].

**Table 2.** LNA circuit parameters

Parameters	PTM 180 nm	PTM 130 nm	PTM 90 nm
$C_{ox} (\text{pF}/\mu\text{m}^2)$	8.6320E-3	10.4638E-3	13.8122E-3
$L_g (\text{nH})$	7.52	7.52	7.52
$L_s (\text{nH})$	0.5	0.5	0.5
$W (\mu\text{m})$	434	496	489
$g_m (\text{A/V})$	0.045	0.045	0.045
$V_{eff} (\text{V})$	0.0618	0.0841	0.037
$I_D (\text{mA})$	1.39	1.894	0.832

### EXPERIMENTAL SETUP AND VALIDATION

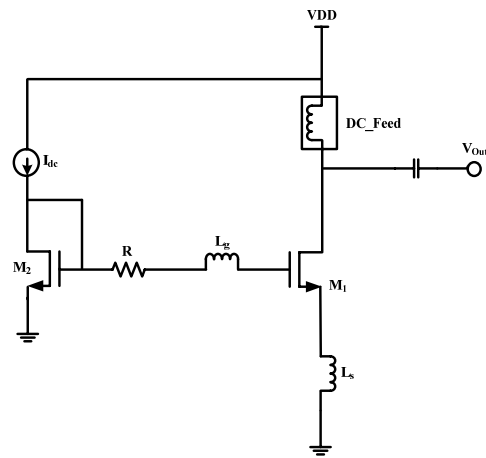
The LNA design with circuit parameter's summarized in Table 2 is modelled in ADS software and a simulation environment is set as shown in Figure 3.

The designed LNA circuit is interfaced with current reference using current mirror and current source. The current mirror circuit is used to avoid extra voltage source in the circuit. The width of MOSFET $M_2$  is set to  $0.1M_1$ , fraction of MOSFET  $M_1$  to minimize the power overhead of the bias current.

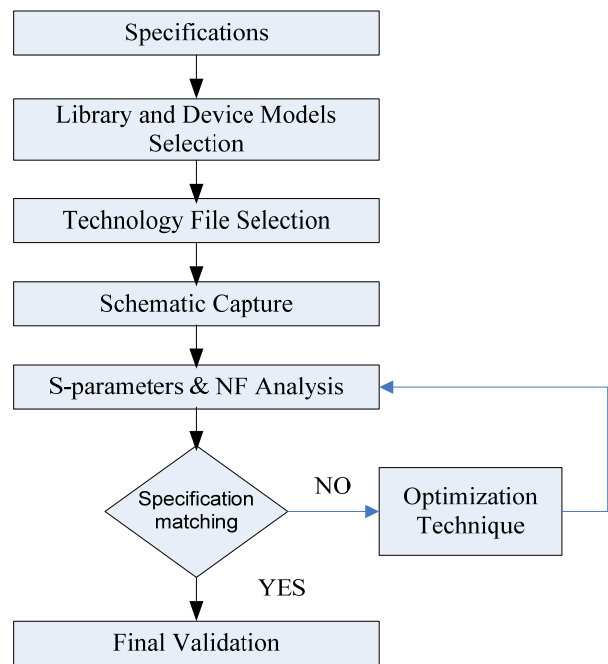
A resistance R is selected so that its equivalent noise current can be ignored. This bias resistor isolates the current mirror from RF input. The capacitors connected between RF input and gate of  $M_1$  and that between drain and output terminal of  $M_1$  are used as DC blocking coupling capacitors. The inductor between drain and supply blocks any RF leaking to the supply rail and may be varied in value to optimize the gain response of the LNA.

A step by step design flow of inductively-source degenerated common source RF LNA using ADS software is shown in below Figure 4. The technology file and device models are selected according to the design specifications. The schematic

of the design is captured by setting the suitable parameters. The design parameters such as s-parameter and NF analysis are checked to meet the design specifications. The optimized LNA is validated and analysed in the following section.



**Figure 3.** ADS simulation setup to analyse the basic LNA design



**Figure 4.** LNA design flow in ADS

### GAIN AND NOISE FIGURE SIMULATION RESULTS DISCUSSION

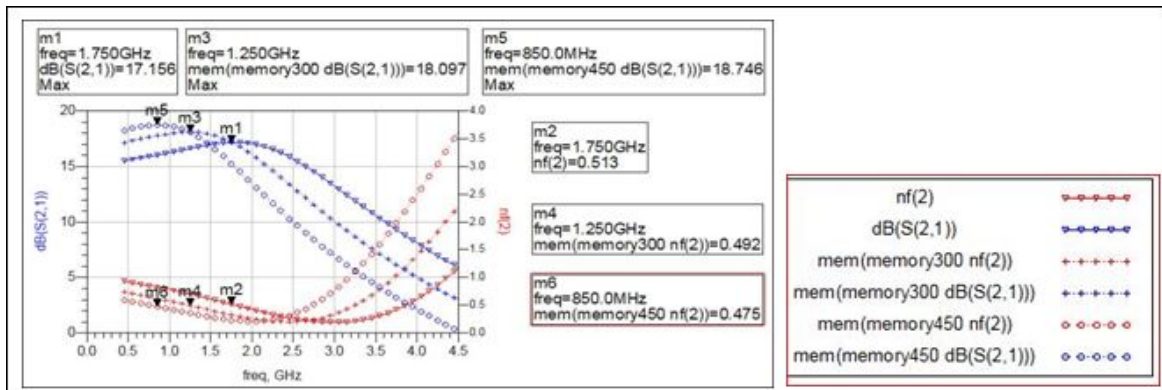
The optimized design of LNA in terms of maximizing gain and minimizing noise figure is considered in this section. Plots of the voltage gain and noise figure with the typical frequency and transistor width with different PTM models are captured and shown in Figure 5 to Figure7 with all the process corners. The different results are summarized in Table3 to Table 5. The maximum gain and minimum noise figure at the centre frequency are reported in Table 6 for MOSFET width of 200  $\mu\text{m}$ .

**A. Power Gain ( $S_{21}$ )**

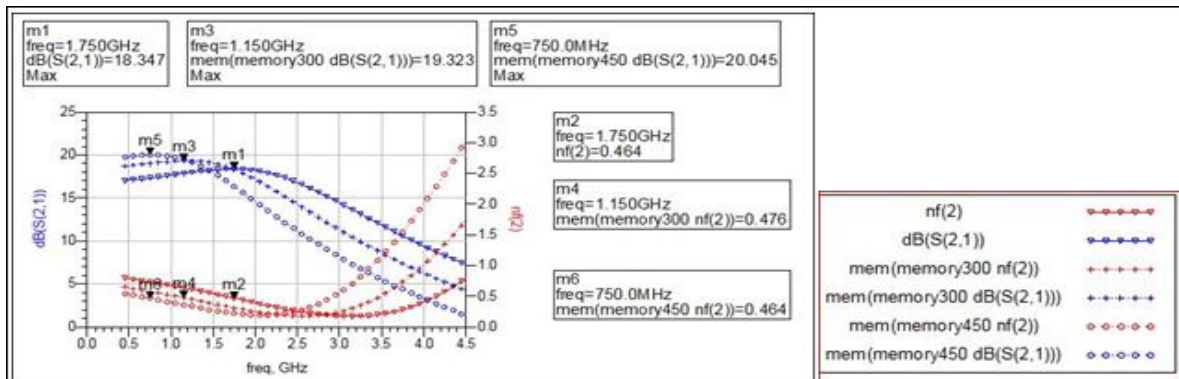
To compensate noise contribution of subsequent stages in the RF receiver of Bluetooth application, it is desirable to have a LNA with power gain ( $S_{21}$ ) more than 10 dB. The inductive degenerated common source LNA with transistor width of  $200\mu\text{m}$  has highest gain of 17.156 dB at 1.75GHz for BSIM 3.1 of  $0.18\mu\text{m}$  technology. At this point the noise figure achieved is 0.513dB. But the gain of 15 dB and the noise figure of 0.223 dB are obtained at the centre frequency of Bluetooth applications. Therefore as the frequency increases the value of gain decreases and improved noise performance. Similar readings are obtained for other PTM models with  $300\mu\text{m}$  and  $450\mu\text{m}$  transistor widths which are presented in Table 3 to Table 5.

**B. Noise Figure (NF)**

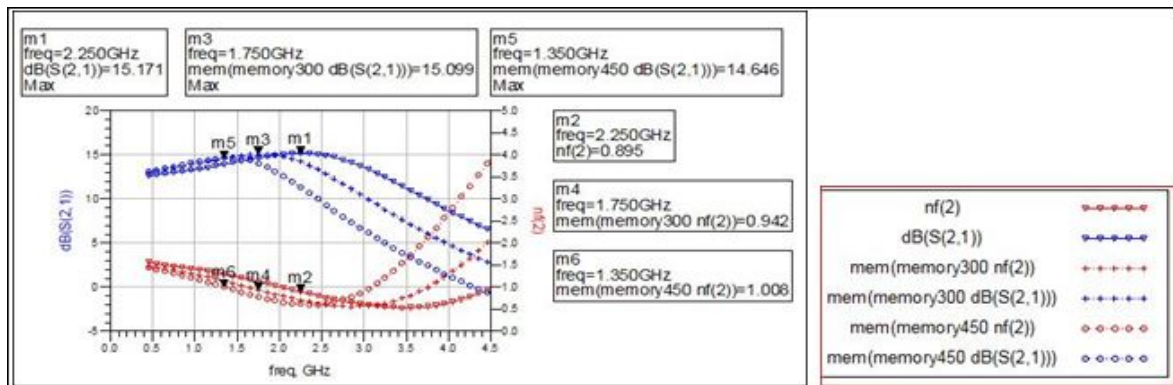
The ADS simulations of the minimum noise figure are obtained from the Figure 5 to Figure 7. The extracted noise figures of the source degenerated LNA are given in the Table 3 to Table 5. For 180nm technology the simulation result indicates the minimum noise figure is 0.189 dB at 2.95GHz with a transistor width of  $200\mu\text{m}$ . At this point the maximum gain obtained is 13.484dB. Similar results are obtained and presented in Table 3 to Table 5 for other PTM models with  $300\mu\text{m}$  and  $450\mu\text{m}$  transistor widths.



**Figure 5.** Maximum gain for PTM 180nm



**Figure 6.** Maximum gain for PTM 130nm



**Figure 7.** Maximum gain for PTM 90nm

**Table 3.** Test case 1 for PTM 180nm model

Parameter	Maximum Gain in dB			Minimum noise figure in dB		
	200	300	450	200	300	450
Width ( $\mu\text{m}$ )	200	300	450	200	300	450
Frequency(GHz)	1.750	1.250	0.850	2.950	2.450	1.950
Noise Figure<2.5dB	0.513	0.492	0.475	0.189	0.198	0.210
Gain ( $S_{21}>10\text{dB}$ )	17.156	18.097	18.746	13.484	13.399	13.807

**Table 4.** Test case 2 for PTM 130 nm model

Parameter	Maximum Gain in dB			Minimum noise figure in dB		
	200	300	450	200	300	450
Width ( $\mu\text{m}$ )	200	300	450	200	300	450
Frequency (GHz)	1.750	1.150	0.750	3.150	2.550	2.050
Noise Figure <2.5 dB	0.464	0.476	0.464	0.168	0.178	0.191
Gain ( $S_{21}>10\text{dB}$ )	18.347	19.323	20.045	13.631	13.941	14.209

**Table 5.** Test case for PTM 90 nm model

Parameter	Maximum Gain in dB			Minimum noise figure in dB		
	200	300	450	200	300	450
Width ( $\mu\text{m}$ )	200	300	450	200	300	450
Frequency (GHz)	2.250	1.750	1.350	3.450	2.850	2.350
Noise Figure <2.5 dB	0.895	0.942	1.008	0.534	0.563	0.609
Gain ( $S_{21}>10\text{dB}$ )	15.171	15.099	14.646	11.428	11.132	10.673

**Table 6.** Gain and noise figure(width W = 200  $\mu\text{m}$ )

Parameter	PTM 180 nm	PTM 130 nm	PTM 90 nm
Gain (dB)	15.00	16.136	14.721
Frequency (GHz)	2.650	2.650	2.650
Noise Figure (dB)	0.223	0.219	0.723

To improve noise figure and gain of common source amplifier with cascode topology can be considered. In addition the device characteristics such as carrier mobility and diffusivity can be considered for design analysis.

## CONCLUSION

In this paper, the design of common source LNA with source degeneration is implemented for different models for Bluetooth applications. The main contribution of this work is the development of the noise modelling of short channel devices for various PTM models. The ADS simulation results indicate that the migration from PTM 180 nm model to PTM 90 nm model there is a frequency improvement of 0.5 GHz, noise figure of 0.382 dB and the gain affected by 1.985 dB for 200  $\mu\text{m}$  width. The migrations from PTM 180 nm model to PTM 130 nm model the noise figure is improved by a factor of 3.25% and the gain is improved by a factor of 6.30% for 300  $\mu\text{m}$  transistor width. Similarly the migrations from PTM 180 nm model to PTM 130 nm model the noise figure is improved by a factor of 2.3% and the gain is improved by a factor of 6.48% for 450  $\mu\text{m}$  transistor width. Therefore the

LNA to operate at maximum gain the recommended technology is 130 nm and transistor width of 450  $\mu\text{m}$ . Similarly the LNA to operate at minimum noise figure the recommended technology is 130 nm and width of 200  $\mu\text{m}$ .

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