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High Performance AXI Protocol Based Improved DDR3 Memory Controller With Improved Memory Bandwidth

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Abstract

The DDR3 Memory has backward compatibility with existing DDR2 Memory and power saving advantage. To increase the performance of DDR3 memory controller, we fire read/write transaction with High speed so require High-speed AXI (Advance extensible Interface) Bus. This paper deals with the high performance AXI protocol based improved DDR3 memory controller with improved memory bandwidth. In this paper, controller clock frequency is 400 MHz and CAS Latency is 10.

Keywords: Prefetch Operation, Refresh Operation, AXI Protocol Interface Block, Data Strobe Signal, Write operation, Measurement of bandwidth

INTRODUCTION

PREFETCH OPERATION:

DDR2 SDRAM uses the 4-bit prefetch operation and DDR3 SDRAM uses the 8-bit prefetch operation [1, 4].

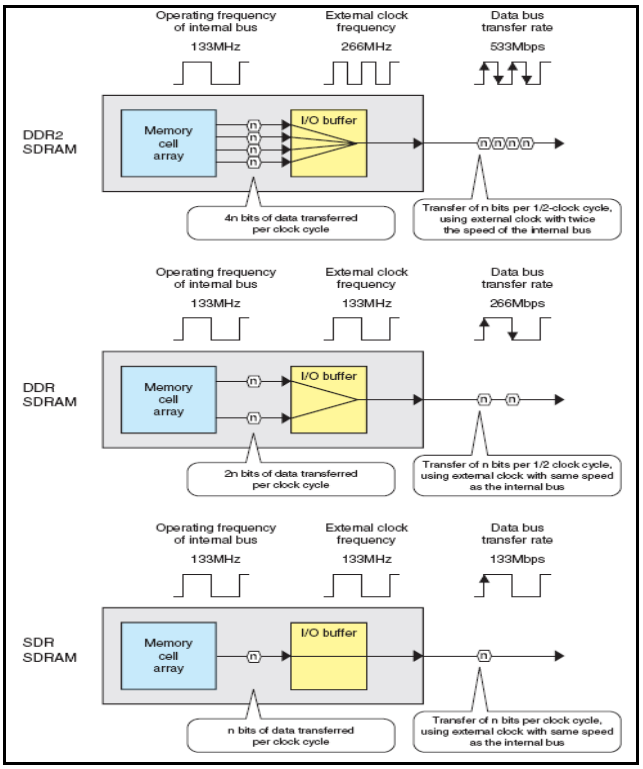


Figure 1.1: 4-bit Prefetch, 2-bit Prefetch and 1-bit Prefetch Operation in DDR SDRAM

Reset:

The Reset pin is used for completely erasing the data in the DDR3 Memory. This is the unique feature available in DDR3 Memory only. This pin should be used with caution because it will remove the complete data [2,3,5].

Data strobe signal in Read cycle:

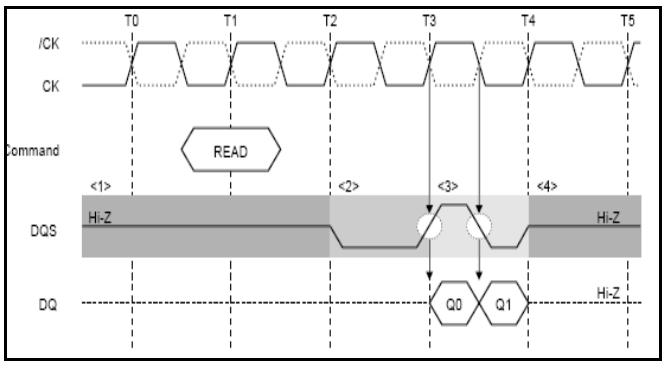


Figure 1.2: shown Read data aligned with DQS signal

Data strobe signal in Write cycle:

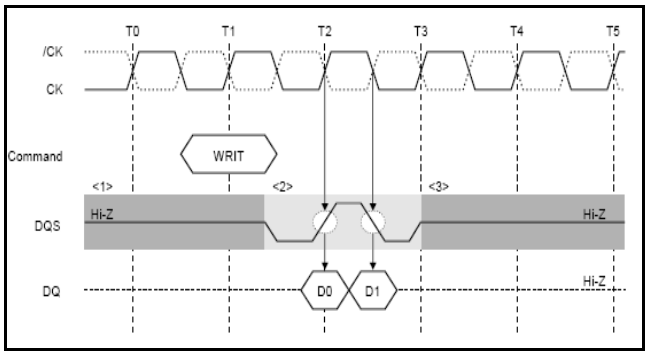


Figure 1.3: Shown Write data aligned with DQS signal

DESIGN METHODOLOGY:

ARBITER OPERATION (AXI PROTOCOL INTERFACE BLOCK)

Arbiter block has two different inputs write and read commands. Polling priority has been used give service to one of these commands [6, 8]. Write command is served

first if AW_LAST of that command is there and command FIFO is not empty. AW_LAST bit decide that complete data is in FIFO means it count the AW_LAST bit and when it is not zero then service write command otherwise not. In the read command case when command FIFO is not empty it will issue read command otherwise not [7, 9, 11].

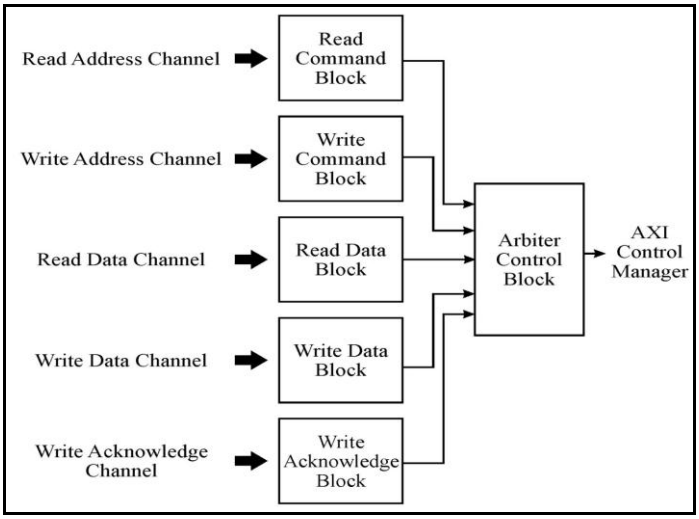


Figure 2.1: Block Diagram of AXI Protocol Interface Block

AXI CONTROL MANAGER :

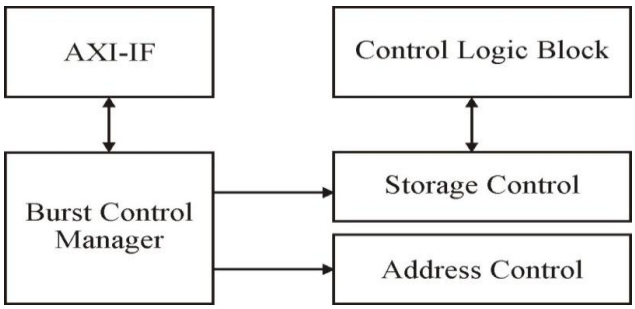


Figure 2.2 Block Diagram of AXI Control Manager

DDR3 Memory Controller: The internal blocks of DDR3 Controller are shown in the figure 2.3.

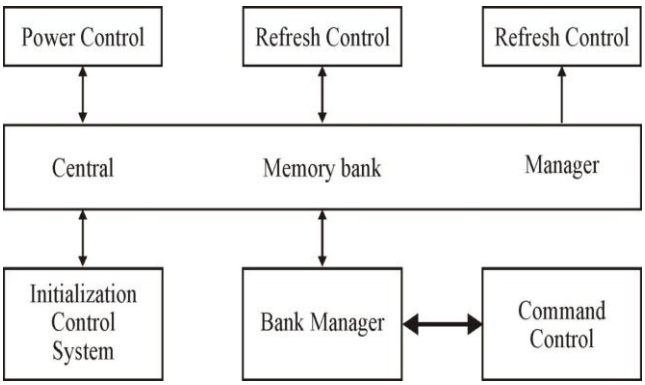


Figure 2.3 Block Diagram of DDR3 Controller Block

Refresh Command:

The 1Gb DDR3 SDRAM requires refresh cycles at an average interval of 7.7256µs (MAX). This command is shown in figure 2.4.

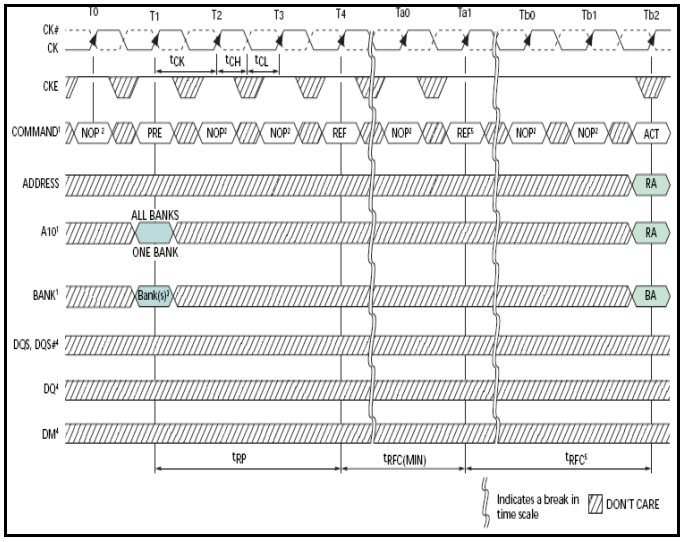


Figure 2.4 Refresh Command

Self Refresh Command:

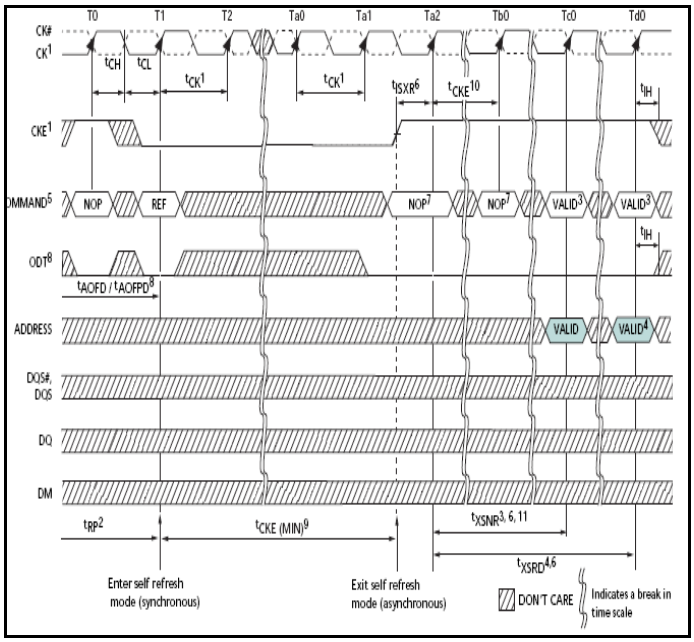


Figure 2.5 Self Refresh Command

SIMULATION, TESTING AND VERIFICATION

The generator fires the random test pattern of random burst size, burst length and addresses, which gets stored in memory in different locations. Memory is used to store the data and different transactions. Monitor block is being used for sampling and driving the input/output of DUT on the AXI

Protocol. Scoreboard is used to trace the error coming in which location and which transaction [12,15].

Refresh Operation:

The DDR3 Memory requires the refresh at an average interval of 7.4 µs. A maximum of eight refresh commands can be posed to any given DRAM [14].

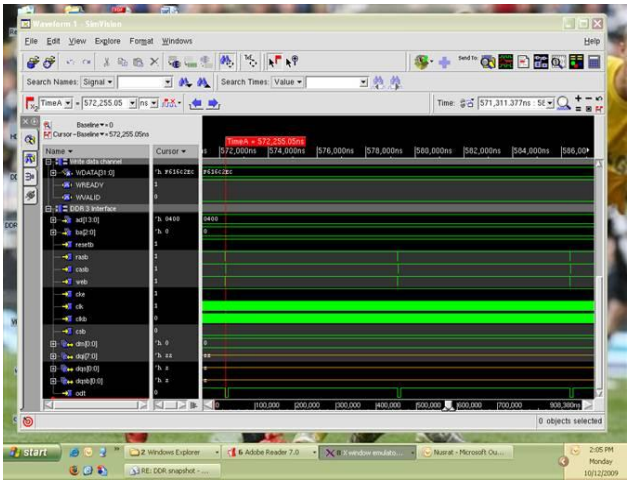


Figure 3.1: Simulation Result of Refresh Operation

Write operation serviced by AXI Protocol Interface block:

When aw_last_in signal is asserted high and write command FIFO is not empty (aw_ready asserted high) then we issue write command and if no read command is there we can issue another write command [5]. The all write commands and data are stored in FIFO when aw_valid and aw_data_valid is asserted high respectively and FIFO is not full. The Results for write operation are shown in Figure 3.2.

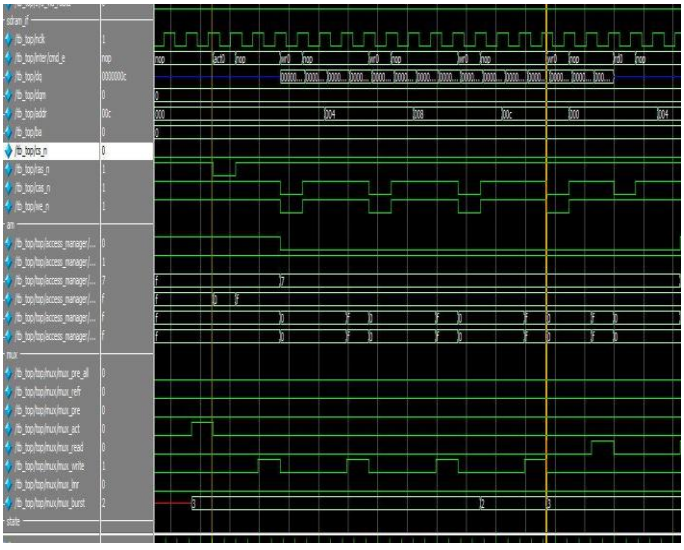


Figure 3.2: Write operation serviced by AXI Protocol Interface block

Read command serviced by AXI Protocol Interface Block:

When read commad FIFO is not empty (aw_ready asserted high) then we issue read command and if no write command is there we can issue another read command. The all read commands are stored in FIFO when ar_valid is asserted high and command FIFO is not full. The read command has higher priority then write command.

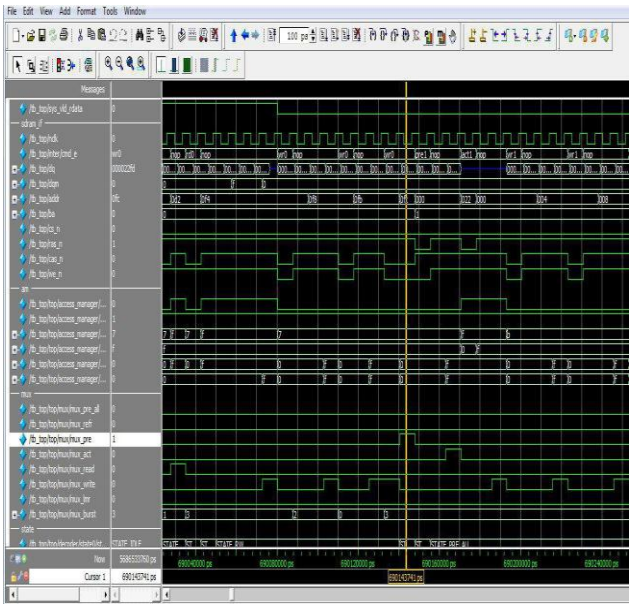


Figure 3.3: Read command serviced by AXI Protocol Interface Block

Write Response of AXI Protocol Interface Block:

Write response channel has three different signals wready, w_response and w_valid_resp_out signal. When we pass write command information to Burst manager block then we also store w_response has OKEY response and when master give wready high then we pass w_valid_resp_out and w_response information to master [8]. In this simulation result shown (in Figure 3.4) w_response, wready and w_vlaid_resp_out signals.

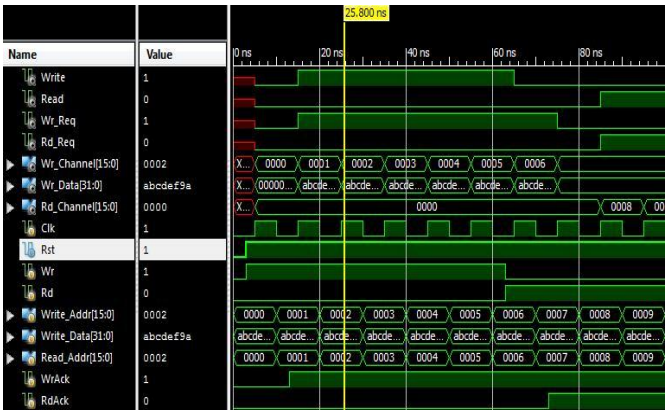


Figure 3.4: Write Response of AXI Protocol Interface Block

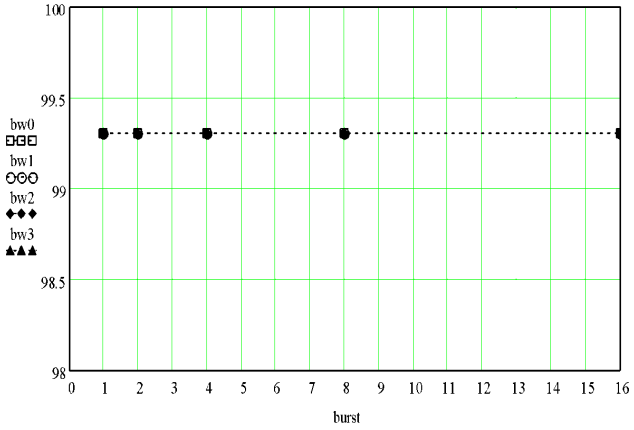
Measurement Results:

Measurement Settings:

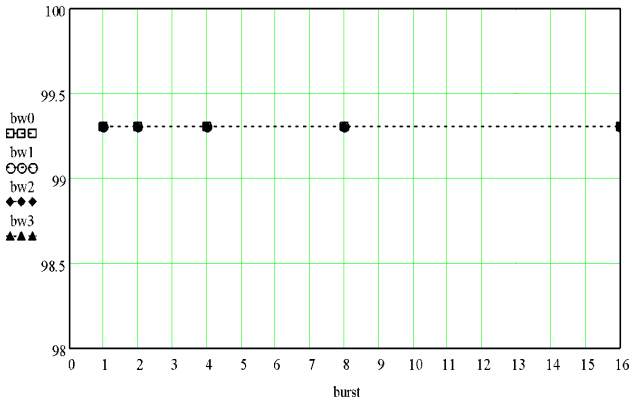
- Measurement Cycle duration: 200us
- Memory refresh interval is 95% of refresh period in 7.8µs.
- Addition bus turnaround cycle is used.
- Transaction Burst Length is 1,2,4,8,16.
- Optimal address alignment is used.
- Controller Clock frequency is 400 MHz.
- CAS Latency is 10.

Measurement results are represented in percentages of maximum memory bandwidth.

- ***Measurement of bandwidth in sequential write mode***



- ***Measurement of Bandwidth in sequential read mode***



CONCLUSION

DDR3 SDRAM core architecture doubles the internal data prefetch from 4n-bit wide transfers to 8n-bit-wide transfers. In DDR3-800 SDRAM, the core array only needs to operate at half the data-rate frequency. However, increasing the prefetch to 8n increases the die size because the internal I/O paths are doubled. With half the data rate frequency, but twice the I/O paths, a DDR3-800 SDRAM has the same core frequency as a DDR2-400 device. In addition to core frequency, DDR2 and DDR3 SDRAM will share a similar migration path. DDR2 SDRAM was defined with 256Mb 4-bank devices at its inception, had 512Mb 4-bank and 1Gb 8-bank devices added for mainstream production, and was eventually developed with 2Gb 8-bank devices for high-capacity memory systems.

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