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The Implementation of Reversible Gates in Design of 1bit, 4-bit ALU and 8b/10b Encoder & Decoder

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Abstract

The implementation of conventional/irreversible logic gates can leads to the high power consumption and also the quantum computation with these logic gates is not possible. The reversible circuits can be used in the digital communication, signal processing, Cryptography as well as in computer graphics. The reversible circuits are the prime requisites for quantum computation where it consumes less gates during the synthesis process and also evolves no redundant input-output line pairs. This paper deals with the design of 1bit, 4bit arithmetic logic controller (ALU) and (8b/10b) encoder and decoder design by using conventional gates and reversible logic gates. The synthesis of the proposed designs were performed by using FPGA and is coded & simulated by using Xilinx 14.7 and modelsim6 respectively. From the performance analysis (by considering propagation delay, quantum cost, garbage outputs and total reversible gates used) it is been found that the proposed designs achieves significant results.

Keywords: Arithmetic Logic Unit, Conventional/Irreversible logic, Decoder, Encoder, Reversible logic, FPGA.

INTRODUCTION

The power dissipation is the major concern in the digital circuit's design or circuit synthesis. The part of power dissipation is technologically related to the non-ideality of the materials and switches [1]. The use of new fabrication mechanisms can reduce the heat loss in the digital circuits. The recent year has witnessed the interest of research domain towards reversible circuits because of its ability to minimize the energy dissipation [2]. This ability of the reversible circuits is the prime requirement in the low power VLSI designs. The applications of the reversible circuits is commonly found in processing of optical information, nanotechnology, low power Complementary Metal Oxide Semiconductor (CMoS) and quantum computation. The irreversible hardware computation leads to higher power dissipation due to information loss [3].

A theory proposed by Landauer [4], states that the energy dissipated (Ed) during the computation by using irreversible gates will be calculated as:

$$E_d = 1.38 \times 10^{23} \times T \times \ln 2 \text{ Joules} \ldots (1)$$

In above eq.(1), the 1.38×10^{23} is Boltzmann constant and its unit is K(joule/Kelvin-1), T is temperature at operation.

Laudauer [4] also suggested the use of reversible can control or eliminate the energy dissipation by bidirectional operation, i.e., the reversible computation will generate the inputs by operation of output and it will return to input at any point of computation. Similarly, the research of Bennet [5] explained that the Ed of eq. (1) will not dissipate until the system generates the inputs from the outputs. The power dissipation can be minimized through reversible computation or lossless reversible logic with bidirectional operation of the system. Thus, this paper aims to implement the reversible gate and proposed SN gate to design 1bit, 4bit ALU and (8b/10b) encoder decoder (with and without reversible gates). The overall paper is categorized: Section 2 explains the concepts of reversible gates, Section 3 gives the operation of proposed SN gate, Section 4 gives design of 1bit and 4bit ALU, Section 5 explains the design and development of 8b/10b encoder with conventional & reversible gates and proposed SN gate. The performance analysis of these two designs was compared with recent designs (Section 6). Finally, the Section 7 concludes the manuscript.

CONCEPTS OF REVERSIBLE GATES

The concept of reversibility is a lossless process, where the un-computed results can be recovered. This reversible process employs the logical process where the energy dissipation is low or no dissipation [1]. The reversible computing mainly helpful in digital logic designs and it offers low powered design with reliability and higher degree of performance. This computing also bring the significant changes in the energy efficiency. The design cost of a digital circuits with reversible logic will be low and hence reversible computing area is considered in research domain [2]. The reversible logic gates (RLGs) exhibit equal inputs as well as outputs and also there will not be any mapping among them. Hence, by using reversible logic the input vectors can be determined with output vectors and vice-versa. In reversibility process some amount of power will be lost and fan-out is not available

which is achieved through an extra gate. Currently, some reversible gates are exist and are expressed below [1-3].

Feynman Gate (FyG)

This gate exhibits two inputs and outputs each. In fig.1, the model of FyG gate is given where inputs (Ip) are P,Q and outputs (Op) are R, S. The output of this gate will be R=P and S=PQ. The quantum cost of this FyG gate is 1 and the gate is utilized as copying gate. Due to unavailability of fan-out, the required output can be duplicated easily [6].

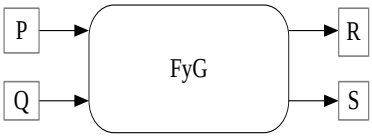

Figure 1. Feynman Gate

Fredkin Gate (FdG)

This gate is of form 3x3, which means it consists of three outputs (R, S, T) corresponding to three inputs (M, P, Q). The model of FdG gate is shown in Fig.2, with inputs and outputs [7]. This gate exhibits the quantum cost of 5 and the outputs can be defined as:

R=M, S=M'P+PQ and T= MP+P'Q where ' indicates the 1s complement.

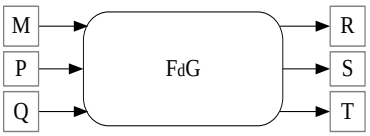

Figure 2. Fredkin Gate

Peres Gate (PrG)

This gate also in the form of 3x3 having mapping outputs R, S, T from the inputs M, P, Q [8]. The input and output of Peres gate (PrG) is represented with Fig.3. The PrG gate exhibits quantum cost of 4 and its outputs can be defined as:

R=M, S= $M \oplus P$ and T= $(M \bullet P) \oplus Q$

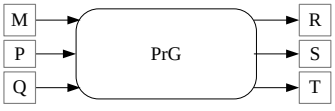

Figure 3. Peres Gate

Proposed SN gate (SNG)

The SN gate is also in the form of 3x3, which uses all the Boolean functions. The following Fig.4, gives the model of proposed SN gate. Here, the outputs corresponding to the inputs are defined as: R=M, S= $M \oplus P \oplus Q$ and T= $(M'P) + MQ$.

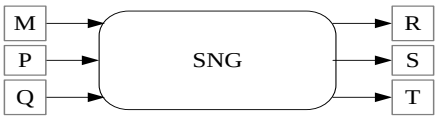

Figure 4. Proposed SN gate

Design of Adders and Subtractors

In the design of the digital circuits, the adders and subtractors plays a major role which performs the addition and subtraction of binary numbers. The addition and subtraction is mainly depends on the control signal. Also, there is a possibility of constructing circuit which performs both addition and subtraction together. The following section discusses the design of adders and subtractors using reversible gates.

Design of Half adder/subtractors

The design of half adder and subtractor is performed by using two reversible logic gates of form 3x3 i.e., proposed SN gate (SNG) and peres gate (PrG). The model of the half adder/subtractors is given in Fig.5 and it has two garbage outputs. In Fig.5, Si or Di indicates sum or difference respectively, carry out of half adder is given with Co while borrow out of half subtractor is indicated with Bo.

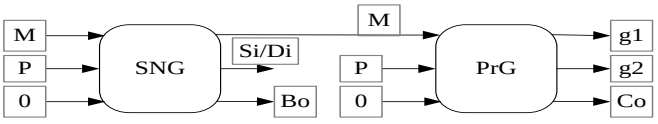

Figure 5. Design of Half adder and substractor

Design of full adder

In order to perform the addition of three binary numbers, full adder is used. Here proposed SNG and PrG is used to design the full adder which realizes the addition operation for M, P and Q. The proposed reversible full adder is shown in Fig.6, having two garbage outputs (g1 and g2). The truth table of this full adder is given in Table.1.

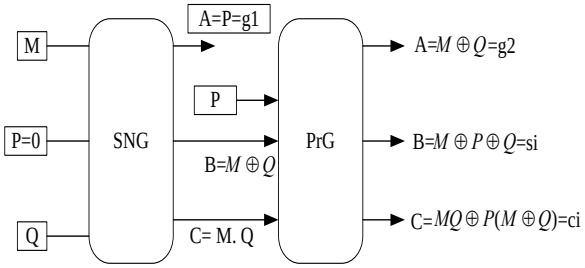

Figure 6. Design of full adder

Table 1. Truth table of full adder

M	P	Q	Si	Ci
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Design of full substractor

In order to perform the subtraction of three binary numbers, full subtractor is helpful as it realizes the subtraction process. For design purpose, Fredkin gate (FrG), PrG and proposed SNG (2 Nos) were used and it generates four garbage outputs (g1, g2, g3 and g4). The following Fig.7, shows the design model of full subtractor and its truth table is given in Table.2.

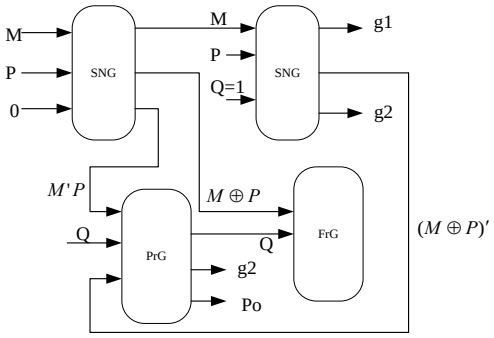

Figure 7. Design of full adder

Table 2. Truth table of full adder

M	P	Q	Di	Po
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Design of 1bit and 4bit ALU

The design of 1bit reversible ALU is synthesized by using Verilog over FPGA. The design of this ALU uses full adder and it does parallel addition. The following Fig.8, indicates the 1-bit ALU design which contains three select inputs like S0, S1, S2 and other inputs like M, P, Q. These signals are given to the full adder which performs addition operation and the gives the outputs like Fi and Cout. The below Table.3, indicates the truth table of 1bit ALU.

Table 3. Truth table of 1bit ALU

S0	0	0	0	0	0	0	0	0	1	1	1	1
S1	0	0	0	0	1	1	1	1	0	0	1	1
S2	0	0	1	1	0	0	1	1	0	1	0	1
Cout	0	1	0	1	0	1	0	1	X	X	X	1
Fi	M	M+1	M+P	M+P+1	M'+P	M⊕P+1	M-P	M	MUP	M⊕P	MxP	M

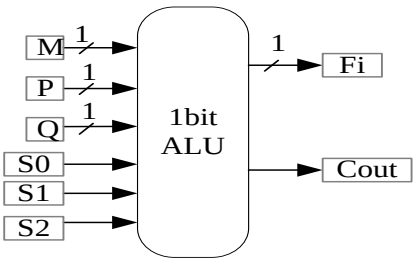

Figure 8. Design of 1bit ALU

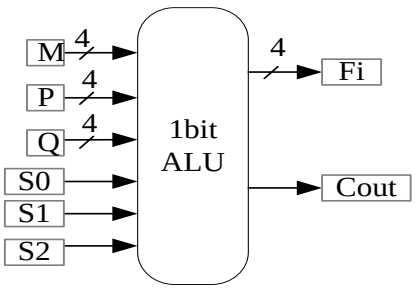

Figure 9. Design of 4bit ALU

Similarly, 4bit ALU is designed by implementing the same concept discussed for 1bit ALU. The Fig.9, indicates the 4-bit ALU design which contains three select inputs like S0, S1, S2 and other inputs like M, P, Q and are called 4-times. These signals are given to the full adder which perform addition operation and the gives the outputs like Fi and Cout.

DESIGN OF (8B/10B) ENCODER AND DECODER BY USING WITH AND WITHOUT REVERSIBLE GATES

The growing industry of the VLSI design demands the low powered devices which can generate the significant performance. But having both low power consumption and steady performance together is a biggest challenge. Most of

the existing research efforts on this challenges were failed to provide optimistic results. The clock gating mechanism can provide the optimization in power usage but consumes higher number of gates. Thus, this paper is involved with the design of 8b/10b encoders with and without reversible gates. Here, two different (8b/10b) encoders and decoders are designed using (i) AND, OR and XOR gate (ii) reversible gates like Fredkin and Peres, (iii) Fredkin and Proposed SNG gate. Finally, the performance analysis of these designs is done to conclude the effectiveness of the proposed SN gate in encoder and decoder design.

In the following Fig.10, the principle of 8b/10b encoding is given in which the 8b data is transferred to 10b data. In the process of encoding, 8b data is divided into two data groups i.e., one of 5b data and another of 3b data. The output of encoding process generates two seperate 4b and 6b data groups to get 10b data. That is, the data lines (ABCDE) of 5b in 8b data (ABCDEFGH) is encoded into 6b lines (abcdei) and the 5b/6b lines directions can be indicated as disparity control and logic functions. Similarly, the 3b lines (FGH) of 8b data (ABCDEFGH) are encoded as 4b lines (fghj). Here, disparity is considered as the difference between the 1's and 0's of a block where 1's represents the positive disparity while 0's indicates the negative disparity. The allowed disparity level among the 6b and 4b blocks will be 0,-2 or +2. The bytes coding concept requires the polarity of non-zero disparity block individually. Hence, the distinction is not introduced between sub blocks of 6b and 4b. This indicates the surplus two (1's) of 6b blocks are compensated through two extra 0's of bidirectional 6b/4b block. Then, the code points of non-zero disparity will be highlighted as complimentary pairs for data points of single source. The parameters of encoding process can leads to the generation of complimentary pairs and for alternate policy rules, the whole sub block is converted as encoder switch. The determination of the polarity and disparity of 6b encoder is done through relevant 4b encoder operations. Finally, the running disparity parameters is forwarded to next 4b encoding operations. Then, the running disparity of the parameter can be given to encoding of next byte. For encoding process, some of the coded sub blocks are of zero disparity and were independent on the running disparity.

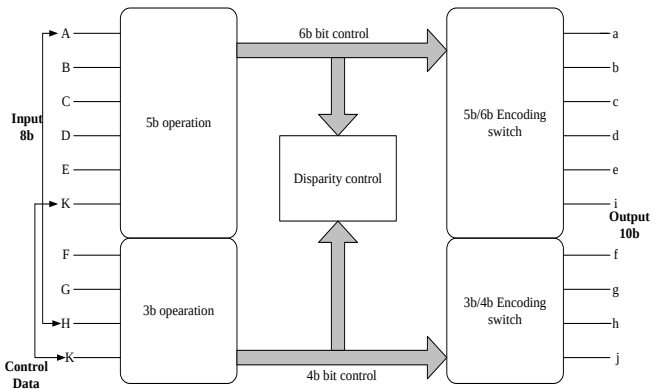

Figure 10. 8b/10b encoder operation

During the decoding process of 10b/8b, the circuits available are used to store the original bytes (ABCDEFGH) and for transmission error representation which is found by transmission code. The decoding is the reverse process of encoding where some changes are introduced by extra circuits to get the faster decoding experience, i.e., 6b/5b and 4b/3b. The above explained encoding and decoding process is implemented in designing the two different 8b/10b encoders and decoders are designed using (i) AND, OR and XOR gate (ii) reversible gates like Fredkin and Peres, (iii) Fredkin and Proposed SNG gate.

RESULTS AND ANALYSIS

This section involves the discussion of results obtained from the execution of the designed adders, subtractors, 1bit, 4bit ALU and 8b/10b encoders and decoders. The synthesis of the designs is performed using Xilinx 14.7 FPGA kit and simulated using modelsim6 simulator.

Performance analysis of adders and subtractors

The proposed 2x2 reversible adder/substractor with peres gate (PrG) and proposed SN gate is compared with the design proposed by Rangaraju et al. [9] that uses four reversible gates (two of FyG and two of FrG). The proposed adder/subtractor generates 2 garbage inputs while the design of Rangaraju et al. [9] generates 3 garbage outputs. Hence, the proposed design is efficient than Rangaraju et al. [9] in terms of garbage output generation. Table 4, indicates the analysis results of reversible half adder/substractor.

Table 4: Analysis of Reversible Half Adder/Half Subtractor

Designs	No. of reversible gates used	Garbage output
Rangaraju et al. [9]	4	3
Proposed design	2	2

The performance analysis of the proposed full adder is done by comparing the designs of Hafiz et al. [10], Rao and Sathyanarayana [11], Khan [12] and Bruce et al. [13]. Full adder of Hafiz et al. [10], used three reversible gates and produces the garbage output of 2. The design of Rao and Sathyanarayana [11] six reversible gates and it generate garbage output of 7 while the designs of Khan [12] and Bruce et al. [13] uses 3 and 5 reversible gates respectively and generates the respective garbage output of 3 and 5. The proposed full adder uses 2 reversible gates and generates 2 garbage output. Table 5, indicates the analysis results of reversible full adder.

Table 5: Analysis of Reversible Full Adder

Designs	No. of reversible gates used	Garbage output
Hafiz et al. [10]	3	2
Rao and Sathyanarayana [11]	6	7
Khan [12]	3	3
Bruce et al. [13]	5	5
Proposed Full adder	2	2

In comparison with the proposed full subtractor design, the reversible gate used in proposed subtractor are 4, in Rao and Sathyanarayana [11] are 6 and in Thapliyal et al. [14] are 5 and the respective garbage outputs of 4, 8 and 9. Table 4, indicates the analysis results of reversible full substractor.

Table 6: Analysis of Reversible Full Subtractor

Designs	Reversible gates used	Garbage output
Rao and Sathyanarayana [11]	6	8
Thapliyal et al. [14]	5	9
Proposed full subtractor	4	4

Performance analysis of 1bit and 4bit reversible ALU

The proposed reversible 1bit and 4bit ALU is used Artix-7 as a FPGA circuit along with devices like XC7A100T and Xc7a100t-3csf324 device, the package is CSG324 and the speed of the device is -3. These helps to calculate the number of gate count; number of garbage and number of constant input used for simulation. The analysis results of 1bit and 4bit ALU is given in Table.6.

Table 6. Analysis of 1bit and 4bit reversible ALU

Designs	Delay (ns)	Quantum cost	Garbage output
1bit ALU of Rangari et al. [15]	6.33	22	8
Proposed 1bit ALU	1.07	22	06
4bit ALU of Rangari et al. [15]	7.885	88	34
Proposed 4bit ALU	3.466	88	10

From the above table.6, it is found that the 1bit & 4bit ALU has least delay, same quantum cost and least garbage output than existing ALU designs of Rangari et al. [15].

Performance analysis of with and without reversible 8b/10b encoder and decoder

This section gives the analysis of the reversible ALU with respect to gates usage by (i) AND, OR and XOR gate (ii) reversible gates like Fredkin and Peres, (iii) Fredkin and Proposed SNG gate. The following Table.7, gives the gate utilization, delay with respect both the designs for encoding and decoding. This indicates the significance of design (iii) over design (i) and design (ii).

Table 7. Analysis of Gate utilization for (i) AND, OR and XOR gate (ii) reversible gates like Fredkin and Peres, (iii) Fredkin and Proposed SNG gate

Type of gate/Parameter	**Encoder**			**Decoder**		
	Design (i)	Design (ii)	Design (iii)	Design (i)	Design (ii)	Design (iii)
Fredkin gate	--	696	256	--	2912	912
Peres gate	--	39	--	--	21	--
Proposed SN gate	--	--	408	--	--	1542
Delay (ns)	1.892	1.926	1.892	3.2	3.052	2.061

CONCLUSION

In this paper, the proposed SN gate is utilized for design of adders and substractors. The same proposed SN gate is used with other reversible gates and designs the 1bit, 4bit ALU and 8b/10b encoder and decoder design (with and without reversible gates). From the results analysis it is found that the adder and subtractor designs were proved significant in terms of reversible gate usage and garbage outputs and is more significant in reversible logic design. Hence, it proved that the design offers initial threshold to develop more complex systems and can execute more complex operations. Similarly the proposed 1bit and 4bit ALU consists of less delay than the existing 1bit, 4bit ALU. Also, garage output and quantum cost refers the significance of proposed 1bit, 4bit ALU than existing one. The results analysis of the (8b/10b) encoder and decoder with respect to conventional gates (design i), existing reversible gates (design ii) and proposed SN gate (design iii) gives that the design (iii) used less number gates than design (i) and (ii) which eventually minimizes the delay as well as area. The design (iii) achieves the improvement in encoder, decoder and encoder-decoder of 9.65%, 16.33% and 15% gates utilization and low delay than respectively in terms of reversible gates used than design (i) and design (ii).

This paper can be further used to build the highly robust communication system like LTE, WiMAX for multimedia communication. For the futuristic research, the proposed paper can be used to bring the security aspects in the communication system with least errors in threat detection.

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