

## DESIGN AND ANALYSIS OF LOW POWER 4 BIT FLASH ADC USING QUANTUM VOLTAGE COMPARATOR

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### Abstract

In the present CMOS technology, Flash ADC is extremely valuable for fastest speed of operation when it is compared with other ADC architectures. The comparators and encoders are the vital part of Flash ADC. The key parameters for analog-to-digital converters are resolution, power consumption and area. Thus in this proposed work, the 4 Bit flash ADC using Quantum Voltage Comparator with priority encoder is designed and analyzed and it is compared with existing ADC's for power consumption and various other parameters. It is analyzed with 0.18 $\mu$ m CMOS technology and simulated using Cadence Virtuoso tool with overall system voltage of 1.8 V. This proposed flash ADC yields SNR value of 6.120 dB with a power consumption of 2.0146 mW and area occupied is 0.021  $\mu$ m<sup>2</sup>.

**Keywords**— Flash ADC, Resolution, power consumption.

### 1. INTRODUCTION

With increase in signal processing and modern communications, handheld wireless computers are becoming more popular. In recent years, mixed integrated circuits are tending towards design of system-on-chip. Flash ADC is often used for high-speed applications. Resolution, speed, power consumption and area are key parameters for an analog-to-digital converter [3].

In proposed Flash ADC, due to its parallel architecture, the application such as high-speed computation and less resolution can be done using the flash architecture. Successive approximation pipelined and sigma-delta modulators are implemented with low power ADC architectures [1]. The increase in the development of utilization

of electrical gadgets like phones, tablets has made power utilization a standout amongst the most prominent design criteria [2].

## 2. RELATED WORK

To know the scope in the area of innovation, development and research, the related work is searched. CMOS technology devices have high resistance to noise and less static power utilization. The speed of the circuit can be increased by designing alteration of Quantum Voltage comparator and 2x1 multiplexer. And flash ADC is simulated with gpdk 180 nm with 25.5 dB SNR and 4.20 mW of power [1]. The research work carried out in [4] explains about the low power, low voltage multiplexer based code converter with high Speed Flash ADC, at the input and output latches of the code converter and using track and hold circuit, the flash ADC is pipelined. The work presented in [5] illustrates the 6 Bit ADC design of a which it has been simulated in 180 nm CMOS technology, the power dissipated is 35.9 mW with +0.019/-0.0199 LSB of DNL and +0.017/-0.022 LSB of INL. In [6] a design of 4-bit ADC with low power and high speed Threshold Inverter Quantization comparator and it is adaptable for variety of applications of System-on-Chip. In [7], 4-bit flash ADC with low power standard cell is proposed. In [8] “Design of a 3.0 MSPS, 2.5 V, 0.25  $\mu\text{m}$ , 4-Bit Flash ADC Based on TIQ Comparator” gives the idea about the designing of 4 bit flash ADC, in which it introduces about multiplexer based design and complete design consume power of 1.9 mW and the 2.99 MS/S sampling rate. The block of comparator consumes power of 354.9  $\mu\text{W}$  from 2.49 V supply.

In this paper, 4 bit Flash ADC in CMOS technology designed with the modification of Quantum Voltage Comparator. Different dynamic parameters have been evaluated.

## 3. INTERNAL BLOCKS OF FLASH ADC

Among the discrete to continuous converters, parallel or flash converters have the highest speed. The block diagram of proposed Quantum Voltage Comparator based 4-bit flash ADC has been shown in Fig.1. It has been divided into 2 parts, quantum voltage comparator array and Priority encoder circuit.

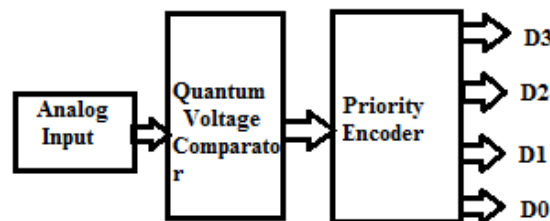


Fig.1 Block Diagram of Flash ADC

### 3.1 QUANTUM VOLTAGE COMPARATOR

The Schematic of quantum voltage comparator consists of differential amplifier and an inverter shown in Fig. 2. By varying the width of transistors and keeping length constant different threshold voltages can be obtained. The output of differential comparator is sent as input to the inverter.

For low power and low voltage applications, flash ADC high lights the Quantized Differential Comparator system [3]. The reference voltages are estimated with input voltages internally, and they are dictated by the sizes of transistor in Quantum Voltage Comparator. The comparator yield will be "1" or "0" based upon applied voltage and threshold voltages. The sizes of transistors are coordinated and the input  $V_a$  is taken from  $V_{ref}$  produced inside. In Quantized Differential Comparator, we design diverse transistor sizes of the transistor M1 and M2. Further, the voltages at  $V_b$  and  $V_2$  are invariant and  $V_1$  is connected as input voltage. By keeping channel length constant and by changing width, the reference voltage is created inside with this deliberate mismatch.  $2^n-1$  distinct sizes of comparators i.e  $2^4-1=15$  comparators for the flash ADC are designed. At the output of the differential amplifier, the inverter is utilized to obtain the Voltage Transfer Characteristic curves.

Single NMOS and single PMOS transistor, with the inverter switching threshold voltage is present in CMOS inverter. By fundamentally differing the widths of transistors, distinctive threshold voltages can be obtained by keeping length of both NMOS and PMOS constant.

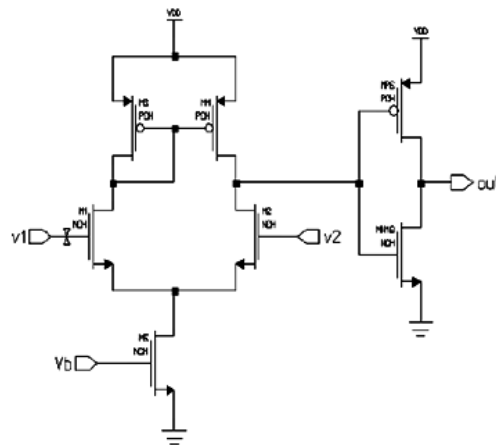


Fig.2 Quantum Voltage Comparator

For theoretical calculations of threshold values the following equation is used. The following equation is derived from resistor string ladder and voltage at each tap is given by

$$V_a = (N * V_{ref}) / M \tag{1}$$

$N$ = Voltage division

$M$ = Number of bits.

$M$ = Total number of resistors.

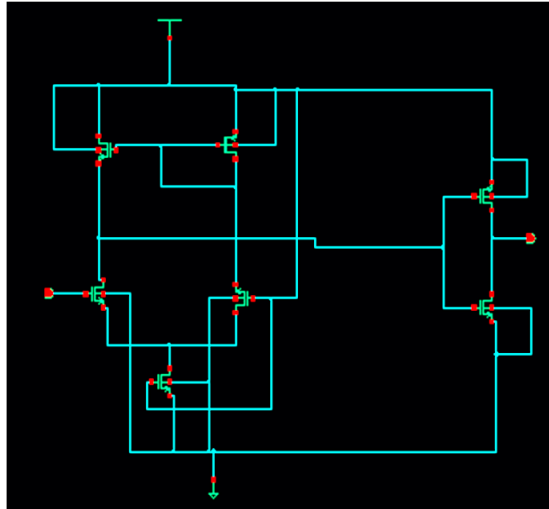


Fig .3 Schematic diagram of Quantum Voltage Comparator

### 3.2 Priority encoder

The comparator yield is in the encoded form. Thus a priority encoder must be outlined keeping in mind the end goal to change over the  $n$  bit encoded signal information (digital) which are unipolar binary code [4] [6]. It is considered as a decision of outline which constricts the yield of comparator which has various binary contributions to discrete outputs [4]. This encoder relies upon the priority of the input. It yields the binary value corresponding to the highest position.

Fig. 4 shows the circuit diagram of Priority encoder and Fig.5 shows the transient response of the same.

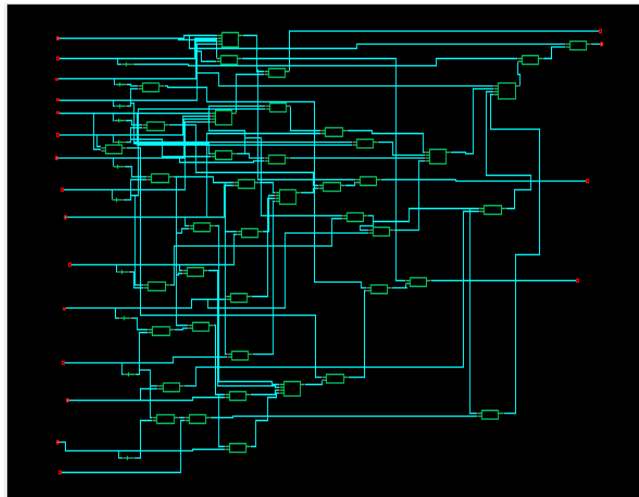


Fig.4 Schematic of Priority Encoder

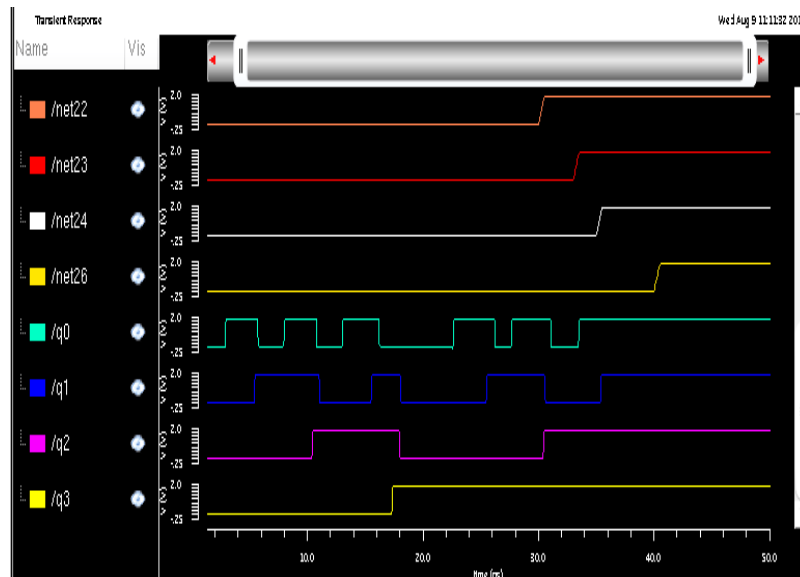


Fig.5 Transient Response of Priority encoder

A priority encoder can be characterized as a circuit that compress numerous binary inputs to fewer output and delivers a yield which is the parallel output of the first number beginning from zero of the most significant input bit. Various sorts of priority encoders incorporate 4 to 2, 8 to 3 priority encoders.

$$04=Q8+Q9+Q10+Q11+Q12+Q13+Q14+Q15.$$

$$03=Q11'Q10'Q9'Q8'[Q4+Q5+Q6+Q7]+Q12+Q13+Q14+Q15.$$

$$02=Q13'Q12'[Q9'Q8'Q5'Q4'Q2+Q9'Q8'Q5'Q4'Q3+Q9'Q8'Q6+Q9'Q8'Q7+Q10+Q11]+Q14+Q15.$$

$$01=Q14'[Q12'Q10'Q8'Q6'Q4'Q2'Q1+Q12'Q10'Q8'Q6'Q4'Q3+Q12'Q10'Q8'Q6'Q5+Q12'Q10'Q8'Q7+Q12'Q10'Q9+Q12'Q11+Q13]+Q15.$$

Table I. Threshold Voltages of QVC

<b>M</b>	<b>Practical Values</b>	<b>Theoretical Values</b>
<b>1</b>	<b>0.1125</b>	<b>0.1123</b>
<b>2</b>	<b>0.225</b>	<b>0.225</b>
<b>3</b>	<b>0.3375</b>	<b>0.338</b>
<b>4</b>	<b>0.45</b>	<b>0.45</b>
<b>5</b>	<b>0.5625</b>	<b>0.56</b>
<b>6</b>	<b>0.675</b>	<b>0.675</b>
<b>7</b>	<b>0.7875</b>	<b>0.788</b>
<b>8</b>	<b>0.9</b>	<b>0.9</b>
<b>9</b>	<b>1.0125</b>	<b>1.0123</b>
<b>10</b>	<b>1.125</b>	<b>1.125</b>
<b>11</b>	<b>1.2375</b>	<b>1.238</b>
<b>12</b>	<b>1.35</b>	<b>1.34</b>
<b>13</b>	<b>1.4625</b>	<b>1.463</b>
<b>14</b>	<b>1.575</b>	<b>1.58</b>
<b>15</b>	<b>1.6875</b>	<b>1.686</b>

#### 4 EXPERIMENTAL RESULTS

The work is carried out in cadence virtuoso and the simulation is done using spectre is shown in this Section .The simulation results of above said two important components of flash ADC is shown. Fig.6 shows the DC response of QVC bank.

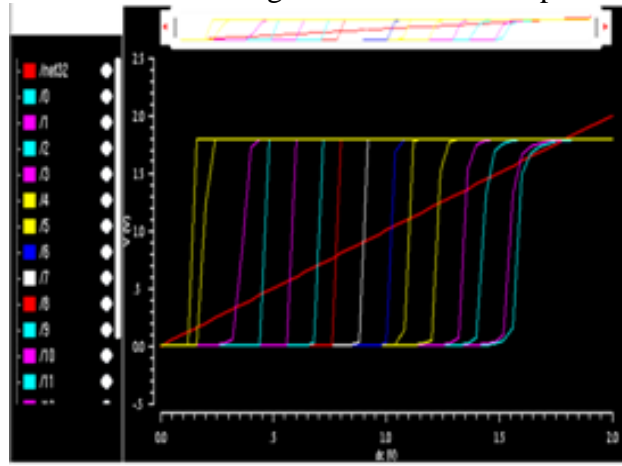


Fig.6 DC Response of QVC Bank

Fig.7 shown below gives the idea about the DC Response of the Flash ADC Using Quantum Voltage comparator circuit

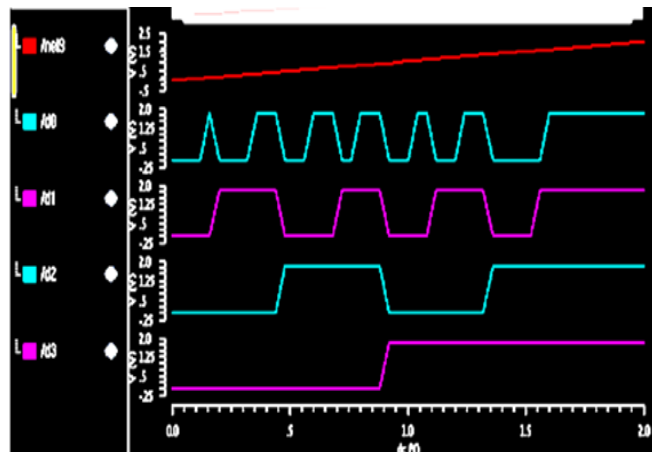


Fig.7 DC Response of Flash ADC

Output of comparator will be at logic ‘0’, as soon as the applied signal voltage is less than reference voltage. The yield of comparator will be at logic ‘1’ when the reference voltage is less than input signal voltage. The comparator gives 15 levels of outputs.

Fig.8 shows transient response for  $V_{in} = 1.4V$ , so here  $V_{in}$  will be in range between  $1.35 \leq V_{in} \leq 1.4625$ , so comparator output will be “111111111111000” and priority encoder output will be “1100”.

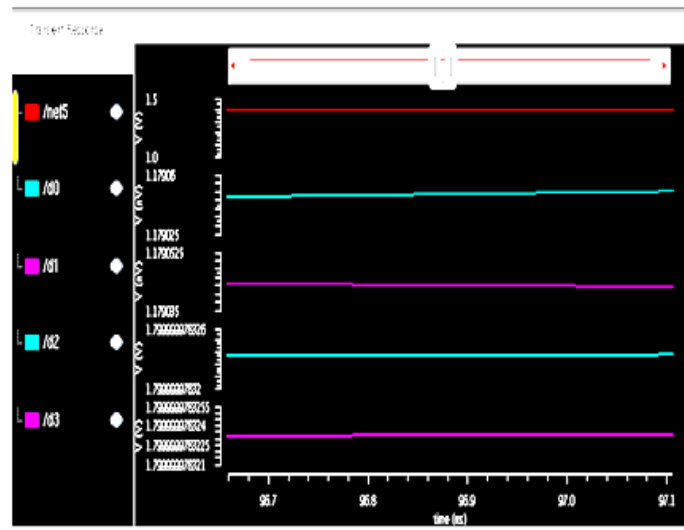


Fig.8 Transient response for  $V_{in}=1.4$ , output will be 1100

Fig.9 shows transient response for  $V_{in} = 0.15V$ , so here  $V_{in}$  will be in range between  $0.1125 \leq V_{in} \leq 0.225$ , so comparator output will be “1000000000000000” and priority encoder output will be “0001”.

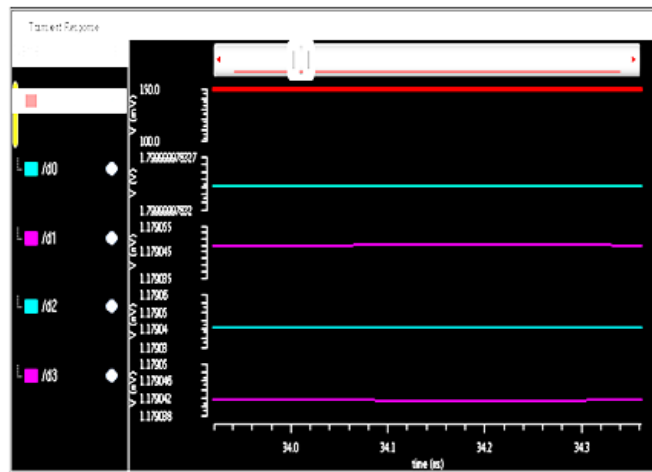


Fig.9 Transient Response for  $V_{in}= 0.15V$  output will be “0001”

## 5. LAYOUT DESIGN

Comparator area is the basic part. Flash ADC gives quickest transformation rate because of its parallel design. It is the key block for fast operation. More power utilization occurs as there is increase in the number of bits. By encoding the thermometer code of an Analog to digital converter is normally changed over into another more minimized and helpful binary code.

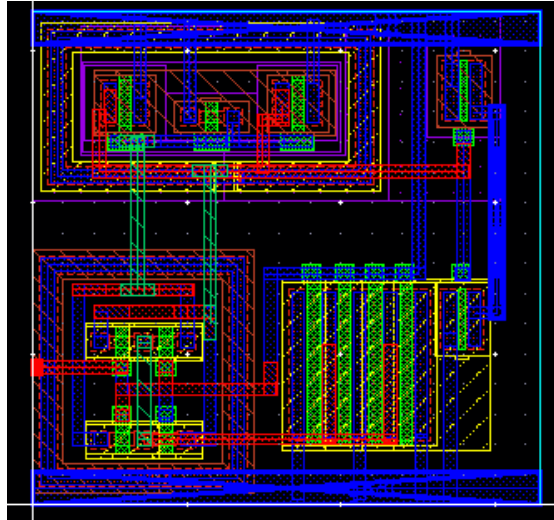
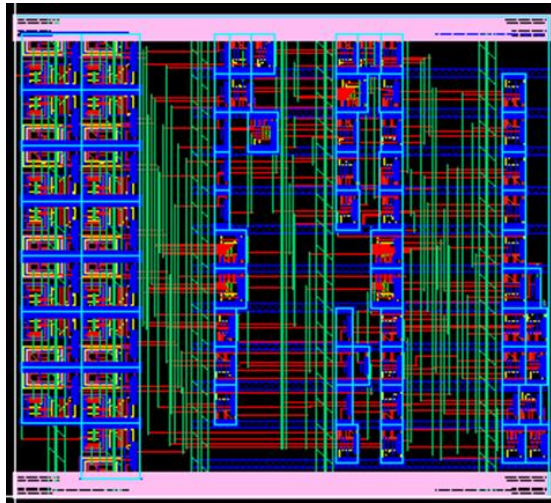


Fig.10 Layout of Single Comparator

X=150.9150um and Y=141.2550um Hence the total area consumed will be  $0.021\mu\text{m}^2$  or  $21.15\text{nm}^2$ .



Comparators Priority encoder circuit

Fig.11 Layout of 4 bit Flash ADC

## 6. OBSERVATION

Table II Comparative study of different flash ADC designs

ADC TYPE	[1]	[2]	[3]	THIS WORK
<b>RESOLUTION (Bit)</b>	4Bit	4 Bit	6 Bit	<b>4 Bit</b>
<b>TECHNOLOGY (nm)</b>	180	90	180	<b>180</b>
<b>SUPPLY VOLTAGE(V)</b>	1.8	1.8	1.8	<b>1.8</b>
<b>POWER(mV)</b>	4.19	4.43	36.98	<b>2.046</b>

## 7. CONCLUSION

The 4 bit flash ADC using Quantum Voltage Comparator is designed and analyzed with 180 nm CMOS technology. The proposed architecture has main advantage of low static power utilization due to the removal of resistor ladder circuit. 2.046mW is the average power consumed by this circuit with SNR value of 6.012 dB and chip area of 0.021 $\mu\text{m}^2$ . ADC is designed and analyzed in standard version – IC 6.1 using Cadence virtuoso tool.

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