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PERFORMANCE COMPARISION OF CONVENTIONAL MULTIPLIER WITH VEDIC MULTIPLIER USING ISE SIMULATOR

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ABSTRACT

Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas).A Multiplier is one of the key hardware blocks in processors. In this paper the implementation of an ancient Vedic Multiplier (VM) for 8 bit x 8 bit is proposed using Urdhva Tiryakbhyam Sutra (UTS). The proposed Vedic multiplier is compared with existing conventional multipliers. Multipliers are coded in Verilog and simulation is done in XILINX software 14.3. Further the performance metrics of multipliers such as area and delay are determined and compared.

Keywords : Vedic Multiplier, Urdhva Tiryakbhyam Sutra.

1. INTRODUCTION

Multipliers are extensively used in Microprocessors, DSP and Communication applications. For higher order Multiplications, a huge number of adders are to be used to perform the partial product addition. The need of low power and high speed Multiplier is increasing as the need of high speed processors are increasing. The Vedic multiplication technique is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems .The mathematical operations using, Vedic Method are very fast and requires less hardware, this can be used to improve the computational speed of processors. The use of Vedic mathematics lies in the fact that it reduces the typical calculations in conventional mathematics to very simple ones.

2. BOOTH MULTIPLIER

It is a powerful algorithm for signed-number multiplication, which treats both positive and negative numbers uniformly. For the standard add-shift operation, each multiplier bit generates one multiple of the multiplicand to be added to the partial product. If the multiplier is very large, then a large number of multiplicands have to be added. In this case the delay of multiplier is determined mainly by the number of additions to be performed. If there is a way to reduce the number of the additions, the performance will get better. Booth algorithm is a method that will reduce the number of multiplicand multiples. For a given range of numbers to be represented, a higher representation radix leads to fewer digits. Since a k-bit binary number can be interpreted as K/2-digit radix-4 number, a K/3-digit radix-8 number. It can deal with more than one bit of the multiplier in each cycle by using high radix multiplication. The flowchart for Booth Multiplier is shown in Fig.1

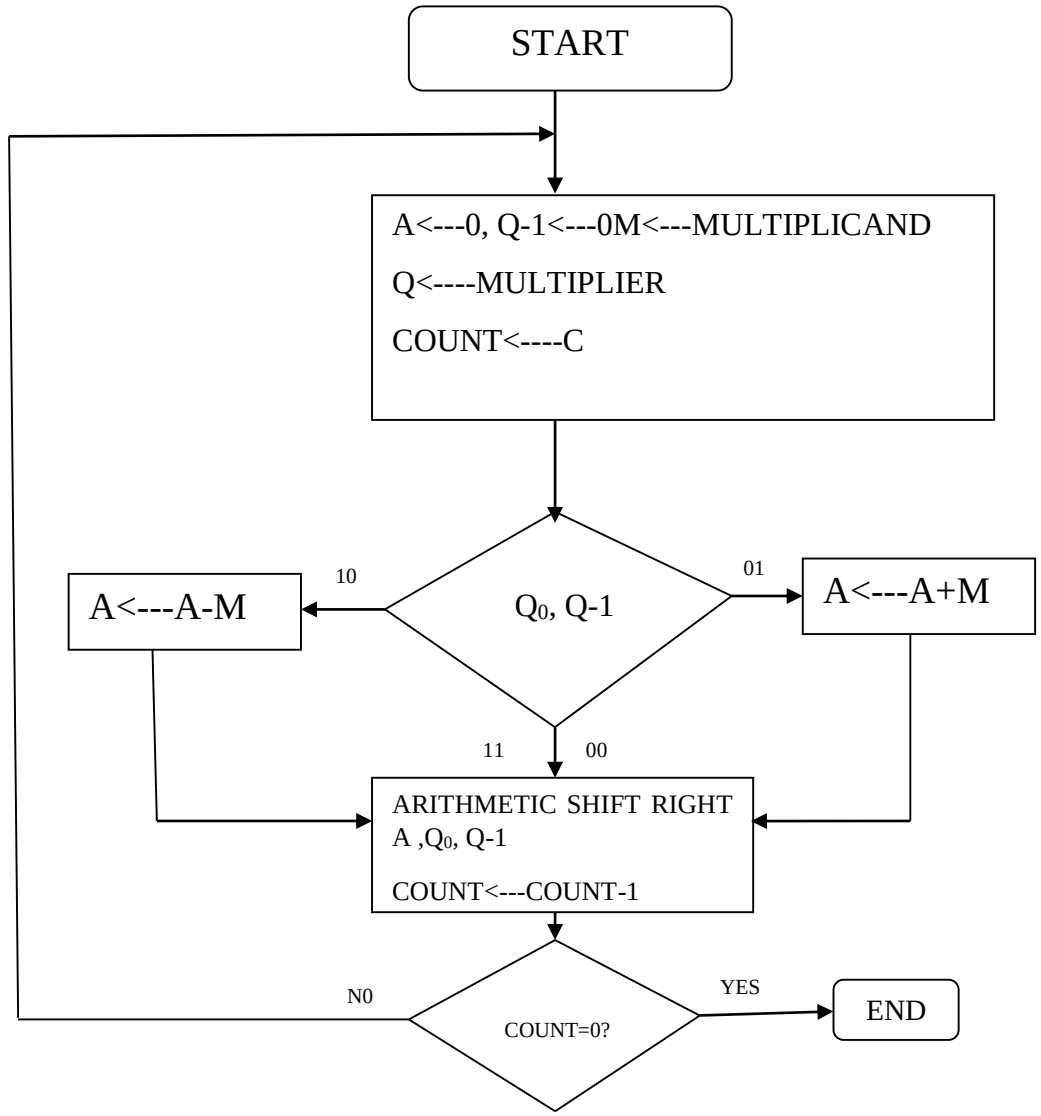

Fig1: Flowchart for Booth Multiplier

This algorithm can be slow if there are many partial products (i.e. many bits) because the output must wait until each sum is performed. Booth's algorithm cuts the number of required partial products in half. This increases the speed by reducing the total number of partial product sums that must take place

3. SIMULATION RESULTS OF BOOTH MULTIPLIER

The Simulation of Booth Multiplier for 4 bit x 4 bit, 8 bit x 8 bit is carried out. The RTL schematic and simulation results for 8 bit x 8 bit Booth Multiplier are shown in Fig.2 and Fig.3 respectively.

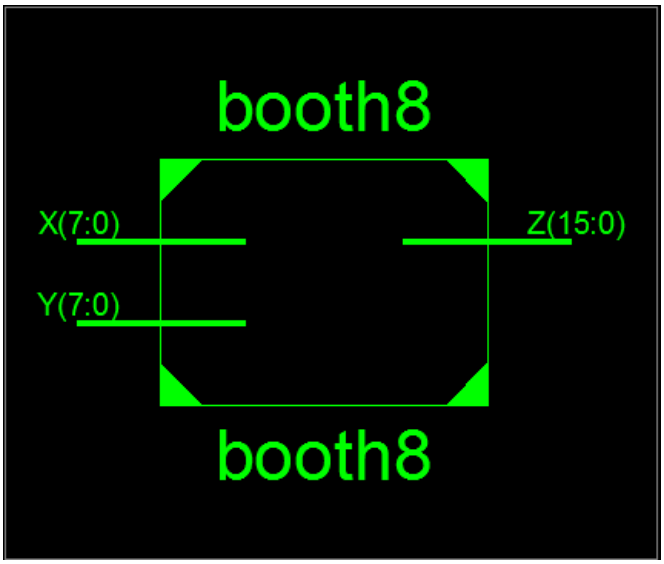

Fig 2: RTL Schematic of 8 bit x8 bit Booth Multiplier

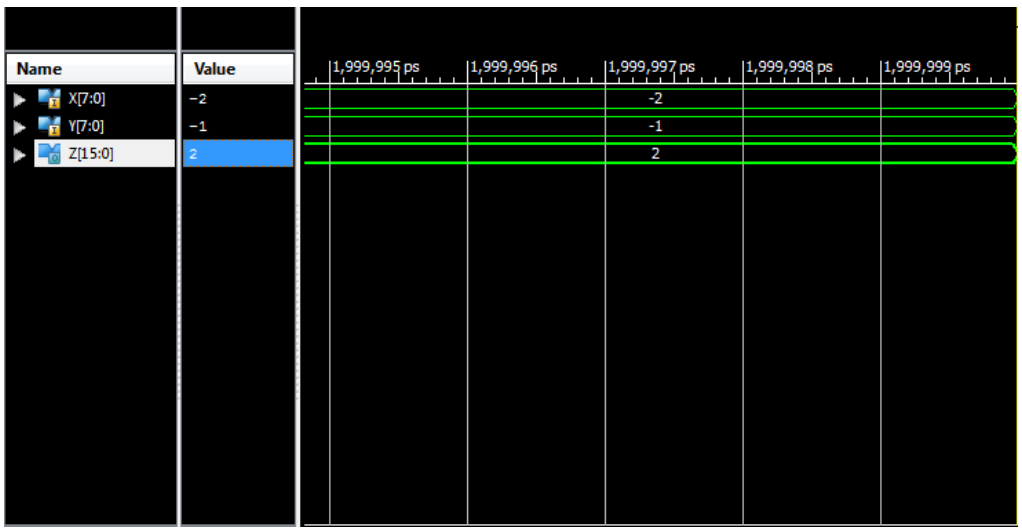

Fig 3: Simulation results of 8 bit x 8 bit Booth Multiplier

4. BAUGH-WOOLEY MULTIPLIER

The algorithm which is having array multiplication for two's complement bits is Baugh and Wooley. The focal point of this multiplier is the sign bits of all the multiplicand and multiplier is unsigned or positive. This algorithm is completely designed by using the conventional logic full adders. Here twos complement numbers multiplied and then finally we get the products as (S0-S7). The multiplication process of Baugh Wooley Multiplier for 4 bit x 4 bit is represented in Fig.4. The similar multiplication pattern is extended for 8 bit x 8 bit.

				A3	A2	A1	A0
				B3	B2	B1	B0
			1	A3B0	A2B0	A1B0	A0B0
			$\overline{\text{A3B1}}$	A2B1	A1B1	A1B1	
		$\overline{\text{A3B3}}$	A2B2	A1B2	A0B2		
	1	A3B3	A2B3	A1B3	A0B3		
S7	S6	S5	S4	S3	S2	S1	S0

Fig 4: 4 bit x 4 bit Baugh Wooley Multiplier

5. SIMULATION RESULTS OF BAUGH-WOOLEY MULTIPLIER

The Simulation of Booth Multiplier for 4 bit x 4 bit, 8 bit x 8 bit is carried out. The RTL schematic and simulation results for 8 bit x 8 bit Booth Multiplier are shown in Fig.5 and Fig.6 respectively

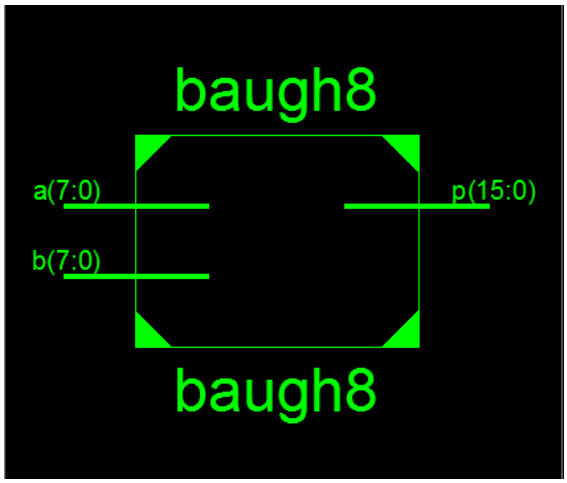

Fig 5: RTL Schematic of 8 bit x8 bit Baugh Wooley Multiplier

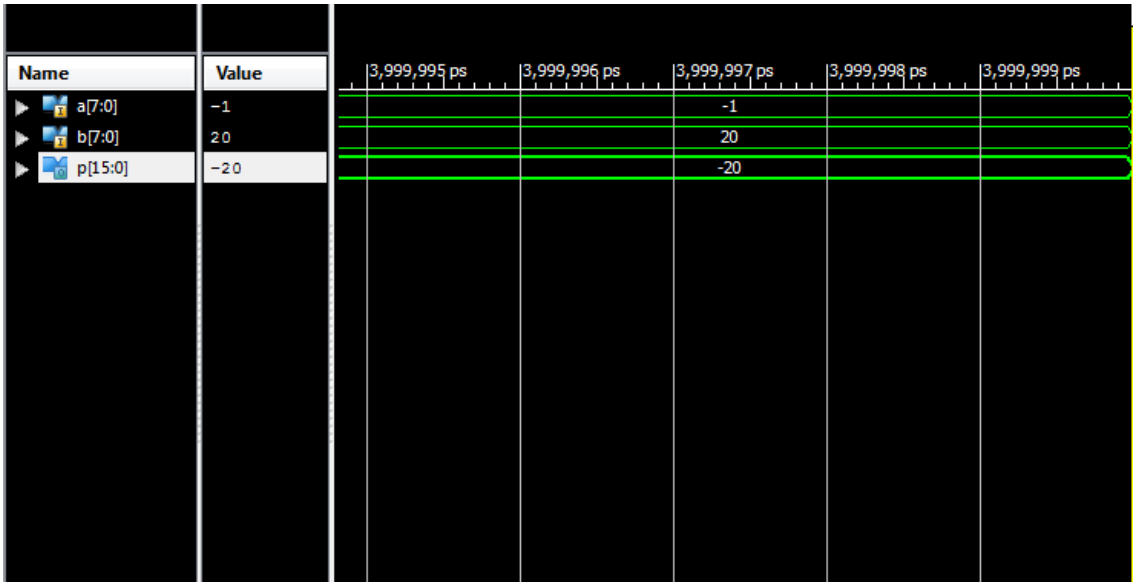

Fig 6: Simulation results of 8 bit x 8 bit Baugh Wooley Multiplier

6. PROPOSED VEDIC MULTIPLIER DESIGN

Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Swami Bharati Krishna Tirthaji Maharaja (1884-1960) after his eight years of research on Vedas. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as sutras. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. Integrating multiplication with Vedic Mathematics techniques would result in the saving of computational time. Thus, integrating Vedic mathematics for the multiplier design will enhance the speed of multiplication operation. The proposed multiplier architecture is based on Urdhva Tiryagbhyam (vertical and cross-wise algorithm) sutra and for partial product addition Wallace tree method is used. The 4 bit x4 bit multiplication has been done in a single line in Urdhva Tiryagbhyam sutra whereas in shift and add (conventional) method, four partial products have to be added to get the result. Thus, by using Urdhva Tiryagbhyam Sutra in binary multiplication, the number of steps required calculating the final product will be reduced and hence there is a reduction in computational time and increase in speed of the multiplier. The steps for 4 bit x 4 bit Vedic multiplier using Urdhva Tiryagbhyam Sutra is shown in Fig.7 and the block diagram for 8 bit x 8 bit Vedic Multiplier is shown in Fig.8. The design starts with the implementation of 2 bit x 2 bit Vedic multiplier. Vedic Multiplier block is then instantiated for 4 bit x 4 bit, 8 bit x 8 bit.

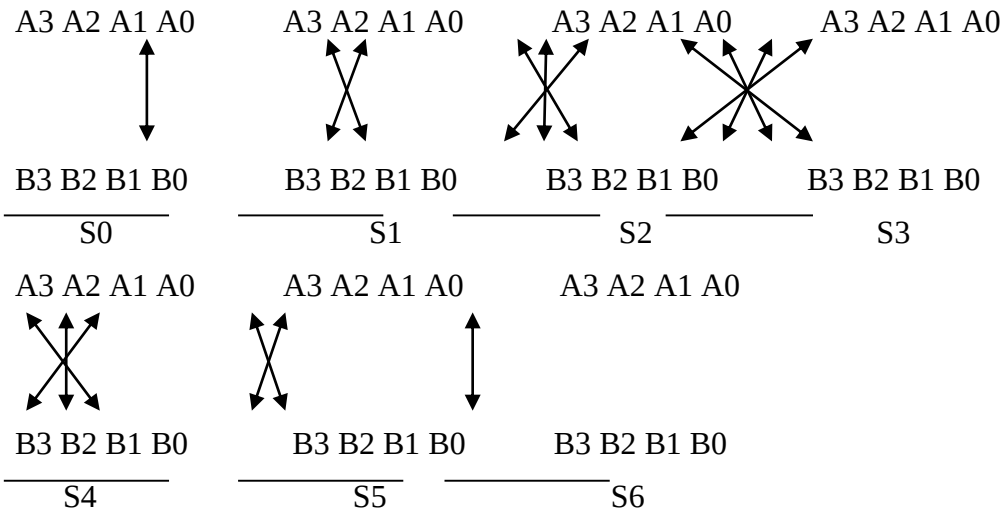

Fig 7: 4 bit x 4 bit Vedic Multiplier using Urdhva Tiryagbhyam Sutra

Step1: S0 = A0*B0

Step2: S1 = A1*B0+A0*B1

Step3:S2 = A2*B0+A0*B2+A1*B1

Step4:S3 = A3*B0+A0*B3+A2*B1+A1*B2

Step5:S4 = A3*B1+A1*B3+A2*B2

Step6:S5 = A3*B2+A2*B3

S**tep7**:S6 = A3*B3

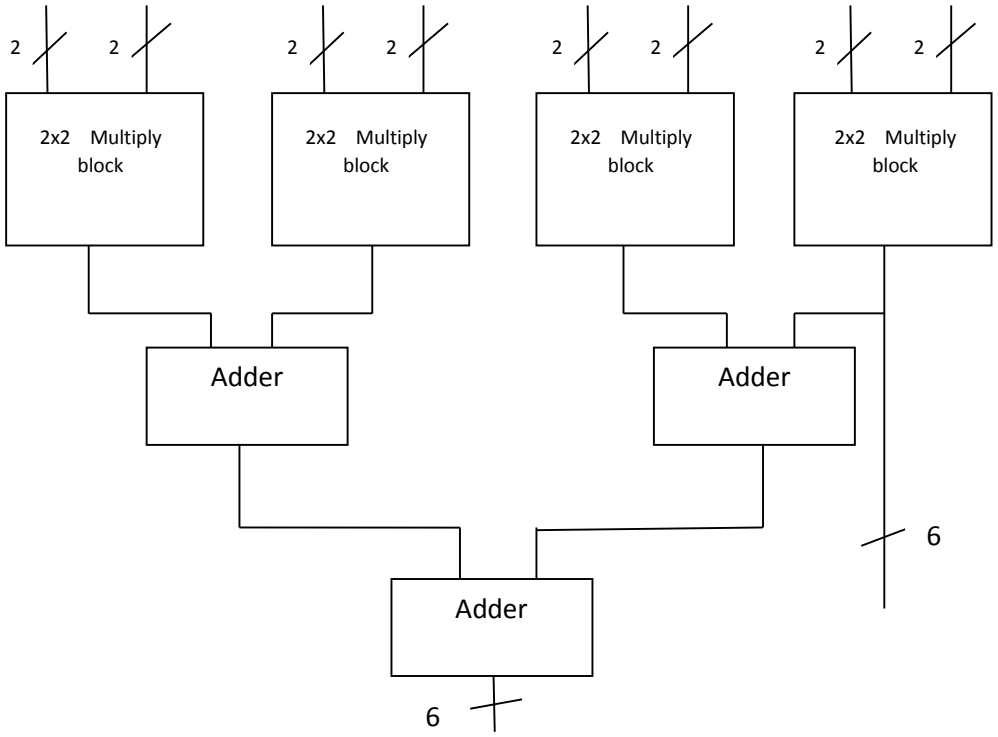

Fig 8: Block diagram of Proposed 8 bit x 8 bit Vedic Multiplier

7. SIMULATION RESULTS OF PROPOSED VEDIC MULTIPLIER

The Simulation of Vedic Multiplier for 4 bit x 4 bit, 8 bit x 8 bit is carried out. The RTL schematic and simulation results for 8 bit x 8 bit Vedic Multiplier are shown in Fig.9 and Fig.10 respectively.

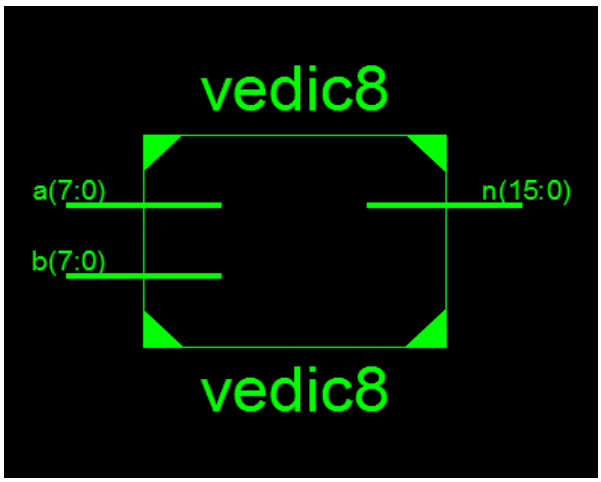

Fig 9: RTL Schematic of 8 bit x8 bit Vedic Multiplier

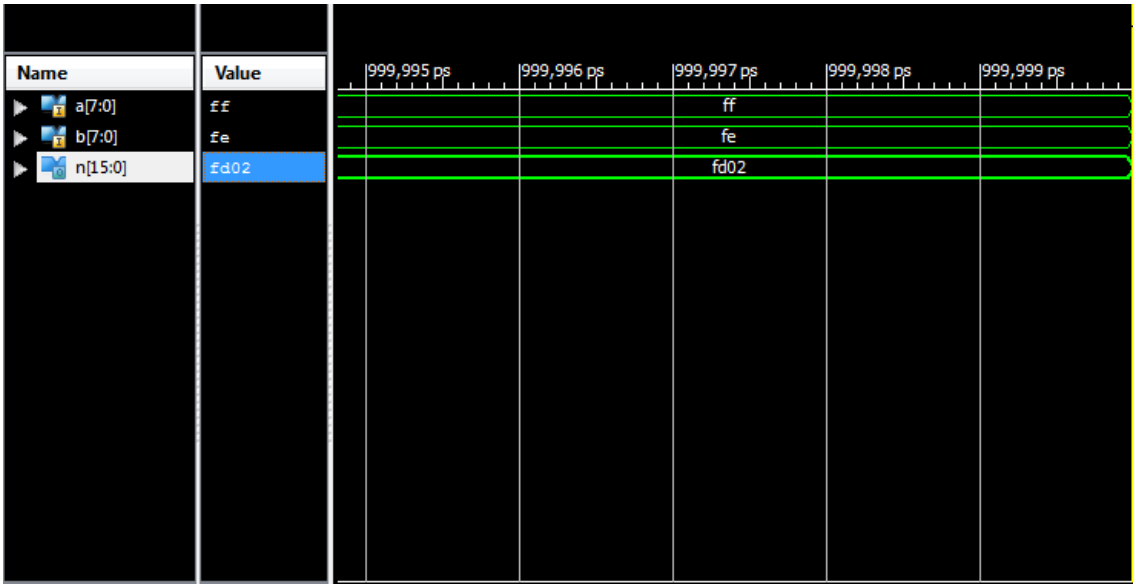

Fig 10: Simulation results of 8 bit x 8 bit Vedic Multiplier

8. COMPARISION RESULTS OF MULTIPLIERS IN TERMS OF DELAY AND AREA

The comparison results of Booth Multiplier, Baugh Wooley Multiplier and Vedic Multiplier are shown table 2 in terms of area and delay for 8 bit x 8 bit.

TABLE 1: Comparison Results

SL.NO	SIZE	DESIGN	LUT'S	SLICES	DELAY(NS)
1	8 bit x8 bit	Booth	139	272	47.23
2	8 bit x8 bit	Baugh Wooley	141	81	29.19
3	8 bit x 8 bit	Vedic	167	96	27.65

9. CONCLUSION AND FUTURE SCOPE

Multipliers are coded in Verilog, simulation is done in XILINX software 14.3. From table 1 it is concluded that Vedic multiplier using Urdhva Tiryakbhyam sutra shows improved performance in terms of delay by 20% when compared to Booth Multiplier and by 2% for Baugh Wooley Multiplier. The area occupied by Baugh Wooley Multiplier is 3% lesser than Vedic multiplier and 16% lesser than Booth Multiplier. The power of Vedic Mathematics can be explored to implement high performance Multiplier in VLSI applications.

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