

## **Analysis of Fabrication Tolerances of Couplers based on Slot Multimode Interference Structures with Arbitrary Power Splitting Ratios**

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### **Abstract**

The optical couplers with arbitrary power splitting ratios using multimode interference structures integrated with slot silicon nanowires have been reported recently. The proposed approach can be useful in designing variable optical couplers and power taps for optical interconnects and optical computing due to its advantages of ease of fabrication, low loss and monolithic integration of electronic and photonic devices on a single substrate. In this paper, fabrication tolerances of such devices are further investigated in detail. The results show that the proposed approach for designing multimode interference based couplers with arbitrary power splitting ratios using slot silicon nanowires can be fabricated with the existing CMOS technology in practice.

**Keywords:** Optical couplers, multimode interference couplers, fabrication tolerance, CMOS technology, silicon nanowires

### **Introduction**

Integrated optical couplers with arbitrary power coupling ratios are important components in optical communication applications. Such couplers are used in Mach-Zehnder interferometer (MZI) structures for optical switches and modulators, power taps, and microresonators, etc. In general, the way to obtain a free choice of the coupling coefficient is to introduce a phase difference at some special positions within the MMI device. The introduction of such a phase shift will lead to new phase relations between the self-images at the output plane.

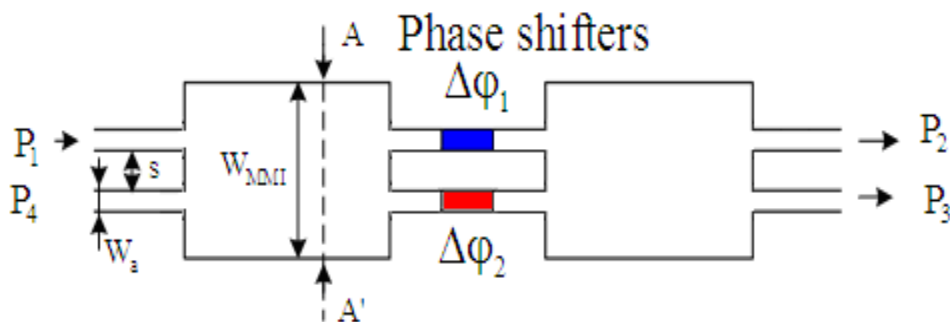
Depending on the material system used for fabricating the MMI coupler, several approaches have been proposed to obtain arbitrary power splitting ratios. One of the most common ways to “tune” the coupling coefficient of a coupler is to use an MZI structure [1]. The tuning of the refractive index using the carrier related plasma effect has been performed directly within the MMI region [2]. The same methods can be applied to the devices designed on other materials but using the thermo-optic effect [3] or the electro-optic effect [4] to change the local refractive index at special locations in the multimode waveguides. The third approach is to use MMI structures having special shapes such as butterfly-like MMIs [5], exponential MMIs [6] and angled MMIs [7], to produce a free selection of the coupling coefficients.

Previous passive approaches for varying the power coupling coefficients of MMI couplers were based on InGaAsP/InP [5] and silica on silicon platform [8] are not suitable for the SOI platform since 3D-BPM simulations were used to simulate these devices and show that the losses are prohibitively high.

Recently, we have shown two approaches for designing MMI couplers with arbitrary power splitting ratios [9, 10]. The first one is to use 1x1 multimode interference coupler as a phase shift element and the second one is to use the slot silicon nanowires. The second approach showed that the low loss and ease of fabrication can be obtained. In this paper, we investigate the fabrication tolerances of MMI couplers with arbitrary power splitting ratios using slot silicon nanowires in detail. The beam propagation method (BPM) is used for this investigation.

## General Theory of Variable MMI Couplers using Slot Silicon Nanowires

The proposed way to achieve arbitrary coupling ratios in MMI structures is to use the canonical structure shown in Fig. 1. Conceptually, it consists of two 3dB restricted interference based multimode interference coupler (RI-MMI) or general interference based multimode interference coupler (GI-MMI) couplers linked by two single mode waveguides that contain phase shifting sections. The idea for using phase shifting sections between MMI couplers was proposed by Yariv [1]. This structure is sometime called the generalised Mach-Zehnder interferometer (GMZI).



**Figure 1:** Schematic of a generalised MZI structure.

Phase shifters are introduced in the linking arms of the MZI to make phase shifts of  $\Delta\phi_1$  and  $\Delta\phi_2$ , respectively. Without the loss of generality, it is assumed that  $\Delta\phi_1 = \Delta\phi$  and  $\Delta\phi_2 = 0$ . The transfer matrix  $\mathbf{M}$  of a 2x2 3dB RI-MMI coupler can be expressed as

$$\mathbf{M} = \frac{e^{j\phi_0}}{\sqrt{2}} \begin{pmatrix} 1 & j \\ j & 1 \end{pmatrix} \quad (1)$$

where  $\phi_0$  is a constant phase and is implied in the following analyses.

The complex amplitudes at the input ports and output ports of the coupler of Fig. 1 can be described in terms of cascaded transfer matrices as

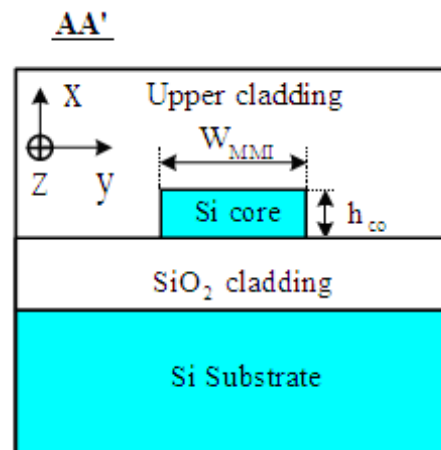
$$\mathbf{S} = \mathbf{M}\Phi\mathbf{M} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & j \\ j & 1 \end{bmatrix} \begin{bmatrix} e^{j\Delta\phi} & 0 \\ 0 & 1 \end{bmatrix} \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & j \\ j & 1 \end{bmatrix} = e^{j\frac{\Delta\phi}{2}} \begin{bmatrix} \tau & \kappa \\ \kappa^* & -\tau^* \end{bmatrix} \quad (2)$$

where  $\Phi$  is the transfer matrix of the phase shift region,  $\Phi = \text{diag}(e^{j\Delta\phi}, 1)$ ,  $\tau = \sin(\frac{\Delta\phi}{2})$ , and  $\kappa = \cos(\frac{\Delta\phi}{2})$ .

For an input signal having power  $P_1$  presented at input port 1 of the coupler in Fig. 1, the powers at the bar and cross ports respectively are given by

$$P_2 = P_1 \sin^2(\frac{\Delta\phi}{2}), \text{ and } P_3 = P_1 \cos^2(\frac{\Delta\phi}{2}) \quad (3)$$

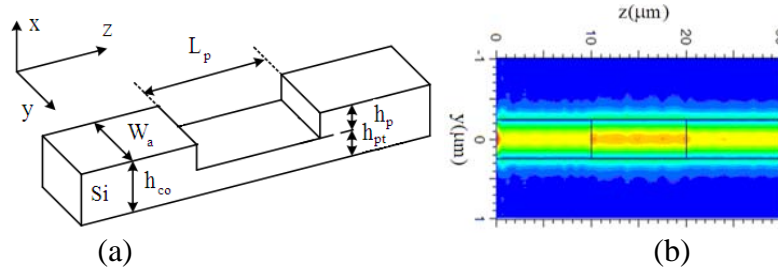
The parameters used in the designs are as follows: the waveguide has a standard silicon thickness of  $h_{\text{co}} = 220\text{nm}$  and access waveguide widths are  $W_a = 0.5 \mu\text{m}$  for single mode operation. It is assumed that the designs are for the TE polarization at a central optical wavelength  $\lambda = 1550\text{nm}$ .



**Figure 2:** Silicon waveguide cross-section used in the designs (the line AA' is shown in Fig. 1)

The approach for making phase shifters on the SOI waveguide is reported. By forming a surface pattern on the top of the MMI region at special positions or on the top of linking waveguides (SOI channel waveguides), any desired phase shift (from 0 to  $\pi$ ) can be produced [10]. The refractive index is adjusted by changing the etch depth, etch width and/or the length of these patterns. The advantages of this approach are that the etching can be done after the device has been fabricated and patterns introduce only low additional loss. In addition, by using suitable masks, only one additional simple process step is required.

The 3D-BPM simulation result (Fig. 3) shows that at a pattern length of  $L_p = 10\mu\text{m}$ , the loss of the signal propagating through the pattern section is only 0.043dB. A pattern depth of  $h_p = 40\text{nm}$  is used throughout this chapter. These dimensions are suitable for practical fabrication.



**Figure 3:** Pattern used for introducing a phase shift (a) structure of the pattern region and (b) power distribution through a pattern having a length of  $L_p = 10\mu\text{m}$

### Analysis of Fabrication Tolerances

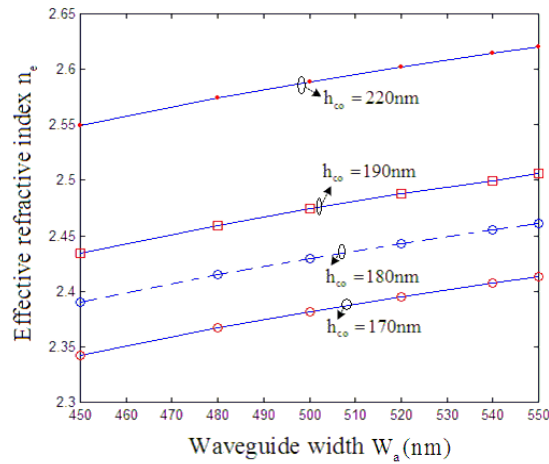
Fabrication tolerances of 2x2 variable MMI couplers using the surface pattern technique is now investigated. Throughout the simulations in this analysis, a pattern depth of  $h_p = 40\text{nm}$  has been used. In practice, such a small etch depth may be very challenging to achieve with precision. Geometrical parameters of the pattern such as pattern depth ( $h_p$ ), shape, width ( $W_p$ ) and length ( $L_p$ ) affect the power splitting ratio. In order to determine the influence of these parameter variations on the power splitting ratio, it is assumed that every pattern region has a rectangular shape and that a pattern region is implemented on the top of the linking waveguides in the MZI structure to produce a phase shift  $\Delta\phi$  (see Fig. 1). The phase shift  $\Delta\phi$  can be calculated by

$$\Delta\phi = \frac{2\pi}{\lambda} \Delta n_e L_p \quad (4)$$

where  $\Delta n_e$  is the difference between the effective index of the standard waveguide (thickness  $h_{co} = 220\text{nm}$ ) and that of the pattern waveguide (thickness  $h_{pt}$ ).  $\lambda$  is the operating wavelength ( $\lambda = 1.55\mu\text{m}$ ).

For simplicity, the influence of geometrical parameters will now be investigated separately and it is assumed that the normalized output powers at the bar and cross ports are determined by equation (3). This means that  $2 \times 2$  3dB MMI couplers in the MZI structure are assumed to be lossless. Such assumptions are possible for investigating fabrication tolerances in this section as only tolerances of the pattern region in the linking waveguides rather than those of MMI couplers will be considered. In addition, this assumption enables the following fabrication tolerance analysis to be applied to the MZI structure using both  $2 \times 2$  RI-MMI and GI-MMI couplers.

Consider an SOI channel waveguide as shown in Fig. 1, where  $\text{SiO}_2$  is used as the upper cladding material. The calculated effective refractive indices  $n_e$  of the fundamental TE mode as functions of different waveguide widths  $W_a$  at a variety of waveguide thicknesses  $h_{co}$  are shown in Fig. 4.

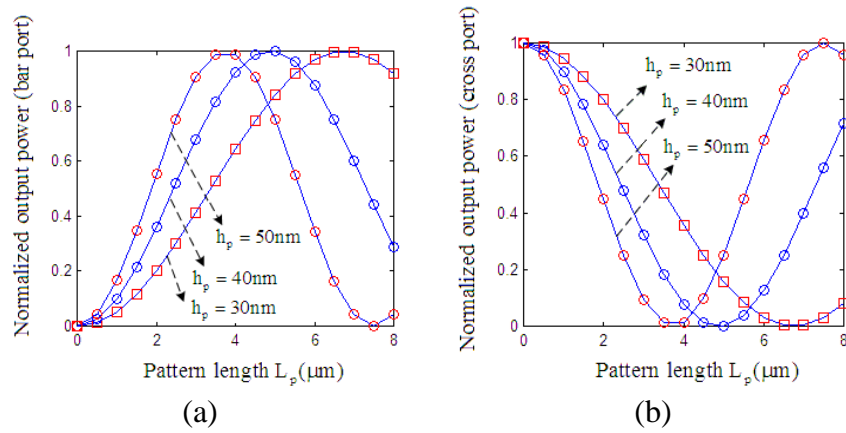


**Figure 4:** Effective indices as functions of waveguide widths at different thicknesses

From these simulation results, it is possible to determine errors in the effective index difference  $\Delta n_e$  for variations of the etch depth and pattern width.

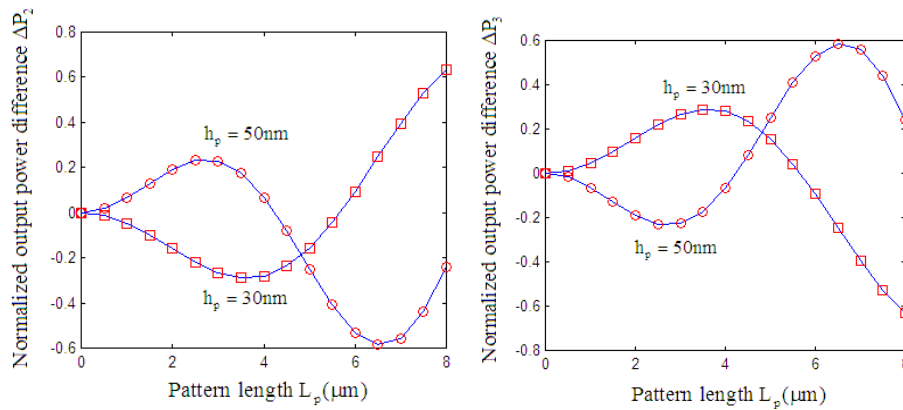
### Thickness variations

Consider an SOI channel waveguide having a width of  $W_a = W_p = 480\text{nm}$  and thickness  $h_{co} = 220\text{nm}$ . The normalized output powers at the bar and cross ports as functions of pattern lengths  $L_p$  for different pattern depths  $h_p$  are shown in Fig. 5(a) and 5(b), respectively.



**Figure 5:** Normalized output powers  $P_2$  and  $P_3$  as functions of the pattern length for (a) the bar port and (b) cross port

The simulation results of Fig. 5 show that the normalized output powers are very sensitive to the pattern depth. The designs for 2x2 MMI couplers in this chapter have been applied to a pattern depth of 40nm. However, it may not be possible to achieve exactly this pattern depth in practice. It is assumed that the fabrication accuracy of the etch depth is of the order of  $\Delta h_p = \pm 10\text{nm}$ . The normalized output powers at the bar and cross ports will change with the pattern depth as shown in Fig. 6(a) and 6(b)



**Figure 6:** (a) Difference of the output powers at different pattern lengths and depths for the bar port and (b) Influence of pattern depths on normalized output powers at different pattern lengths for the cross port

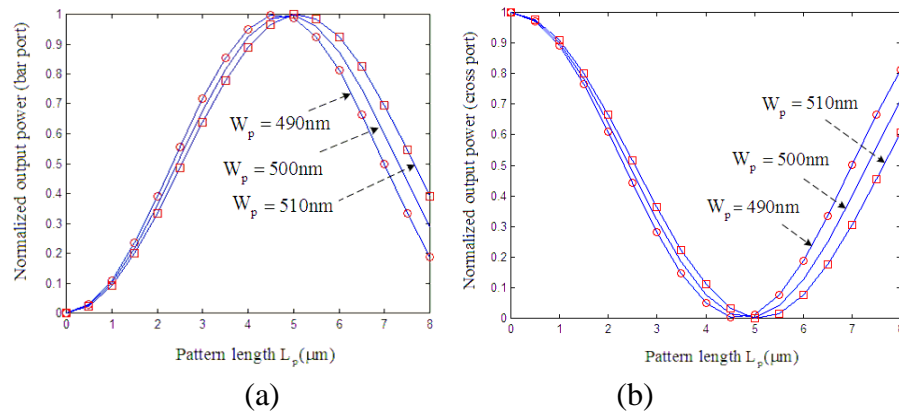
Here the normalized output power difference  $\Delta P_2$  for the bar port and  $\Delta P_3$  for the cross port are the differences between the normalized output powers (at the same port) at the pattern depth  $h_p$  and those at the pattern depth of 40nm.

It has been shown that a maximum pattern length of around  $5\mu\text{m}$  is sufficient in order to achieve the power coupling ratio over the range from 0 to 1. The simulations (Fig. 6) show that if a pattern length is less than  $5\mu\text{m}$ , then maximum variations of the normalized power difference are  $\mp 0.25$  for fabrication tolerances of  $\pm 10\text{nm}$ . It is noted that the difference of the normalized output powers will change significantly if the pattern length increases (more than  $5\mu\text{m}$ ). Therefore, it may be useful to fabricate the pattern region having as a short length as possible.

One possible way to reduce the effect of the etch depth error is to later separately etch another pattern region in the other linking waveguide in the MZI structure so that the phase error due to the initial fabrication error in the first linking arm is compensated. However, this further process may require expensive equipment.

### Waveguide width variations

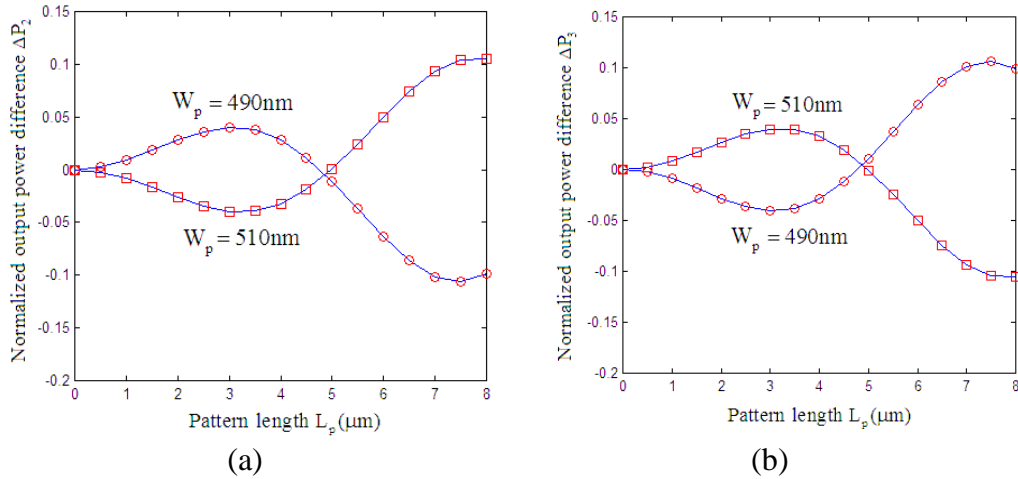
The influence of pattern width ( $W_p$ ) variations on the normalized output powers will now be considered. The SOI channel waveguide having a thickness of  $h_{\text{co}} = 220\text{nm}$  and waveguide width of  $W_a = 500\text{nm}$  is used. It is assumed that the pattern depth  $h_p$  is kept unchanged at  $h_p = 40\text{nm}$ . The normalized output powers at the bar and cross ports as functions of the pattern length with different pattern widths are shown in Fig. 7(a) and 7(b), respectively. The simulations show that a change in the pattern width will affect the normalized output powers, particularly when the pattern length is longer than around  $5\mu\text{m}$ , but to a less degree than the pattern depth.



**Figure 7:** Normalized output powers as functions of pattern lengths at different pattern widths for (a) the bar port ( $P_2$ ) and (b) cross port ( $P_3$ )

Pattern width variations of  $\pm 10\text{nm}$  will cause the normalized output powers at the bar and cross ports to change as shown in Fig. 8(a) and 8(b). If the pattern length is less than  $5\mu\text{m}$ , then maximum power differences at the bar port  $\Delta P_2$  and at the cross

port  $\Delta P_3$  both are 0.1. This means that the effect of waveguide width tolerances is much smaller than that of etch depth tolerances. Also, it has been shown that the accuracy of fabricating the etch depth is directly proportional to waveguide widths [11]. Therefore, it may be desirable to use wide single mode waveguides to relax the tolerance on the etch depth.

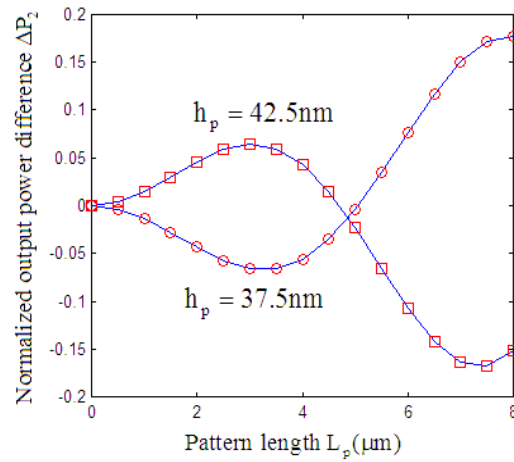


**Figure 8:** Influence of pattern depths on normalized output powers at different pattern widths for (a) the bar port and (b) cross port

In conclusion,  $2 \times 2$  MMI couplers with arbitrary power splitting ratios on the SOI channel waveguide using the surface pattern technique are achievable. However, the normalized output powers are very sensitive to the pattern depth and width. In practice, it is extremely difficult to fabricate a particular pattern precisely. Variations in the fabrication process such as control of etch depth uniformity, etching profile and process control of waveguide width need to be taken into account. A fabrication accuracy of 10nm can be achieved by using 248nm deep UV lithography [12, 13], which has been used for fabricating several optical devices on silicon channel waveguides. It is also possible to achieve a smaller fabrication accuracy (for example around 5-10nm [14]) using e-beam lithography which has a very high resolution [15] or 193nm deep UV lithography [16] and multiple-step etch process [17]. Disadvantages of these technologies are that they are more costly and not so suitable for quantity production.

For example, if the fabrication tolerances for etch depth are  $\Delta h_p = \pm 2.5\text{ nm}$ , then the normalized output power difference  $\Delta P_2$  for the bar port at these fabrication tolerances is shown in Fig. 9. Here, the desired pattern depth is  $h_p = 40\text{ nm}$ .





**Figure 9:** Normalized power difference at the bar port as a function of the pattern length for pattern depths of 42.5nm and 37.5nm

It is clear from Fig. 9 that the maximum value of the normalized power difference  $\Delta P_2$  is 0.12 when the pattern length  $L_p$  varies from 0 to  $5\mu\text{m}$ . It can also be seen from this simulation that the normalized power difference will increase when the pattern length is around  $2.5\mu\text{m}$ , that is when a power splitting ratio of 50/50 is expected. Therefore, the designer must take care more when power splitting ratios of around 50/50 are needed using the surface pattern technique.

The simulations have shown that the pattern length must not be very long (less than  $5\mu\text{m}$  if  $\text{SiO}_2$  is used as the upper cladding material) to reduce fabrication errors. A way to reduce errors in etch depth is to use one more pattern region in the other linking waveguide to compensate for the error. This method is possible since the pattern region can be implemented after devices are fabricated.

Another way to improve control of the etch depth precisely is to use real-time control combined with run-to-run control as proposed by Hankinson et al. [18]. This approach has been demonstrated in high-aspect-ratio etching in SOI wafers and can provide the real-time process analysis. Hence, fabrication accuracy can be improved significantly.

The above approaches for improving fabrication accuracy may enable the surface pattern technique to be employed in practice. The proposed approach does not require more real estate. The method is particular useful for achieving power splitting ratios required for critical coupling in MMI-coupled microresonators for photonic signal processing applications.

## Conclusion

The fabrication tolerances of multimode interference couplers with arbitrary power splitting ratios using slot silicon nanowires has been investigated in detail in this

paper. The beam propagation method was used for the analysis. The results have shown that the proposed approach for designing variable couplers can be implemented easily with the existing CMOS technology in practice.

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