

## DOCCCII based Configurable Analog Block Design for FPAA Implementation in 16nm Technology

\*Sadia Shireen<sup>1</sup>, Mohd.Faseehuddin<sup>2</sup>, M.Y.Yasin<sup>3</sup>

<sup>1&2</sup>M.Tech Students, <sup>3</sup>Asst. Prof., Electronics & Communication Department,  
Integral University, Lucknow, India

<sup>1</sup>sadiashireen53@gmail.com <sup>2</sup>faseehuddin03@gmail.com

<sup>3</sup>mmyasin@rediffmail.com

### Abstract

Field programmable analog array (FPAA) is the rapid emerging technology for hardware prototyping of analog applications where low power, small design time and low design cost are required. Its requirement of less area and reduced power makes it more efficient than digital counterparts. In this paper we propose a 2<sup>nd</sup> generation Dual output current controlled current conveyor (DOCCCII) in 16nm bulk CMOS technology using PTM (High Performance 16nm Metal Gate / High-K / Strained-Si parameters published by the Arizona State University, USA) and discuss its dynamic characteristic. A configurable analog block (CAB) is also proposed, which mainly consists of a DOCCCII and minimum number of MOSFET switches, to make it readily configurable to realize analog applications. This CAB is used for realization of the integrators and differentiators. The CAB is versatile enough to realize different second order function involving systems like filters and oscillators. Performance of the CAB based realization is compared with their normal realizations. The results of comparison are quite satisfactory.

**Keywords**— DOCCCII applications, Electronically tunable design, Configurable Analog Block, Field Programmable Analog Array.

### Introduction

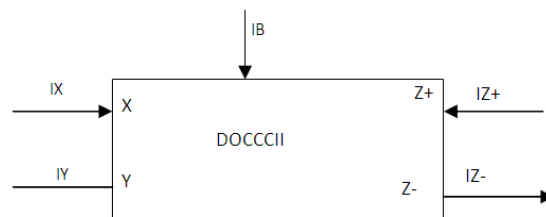
So far, digital VLSI has generally enjoyed a dominant market share, whereas the analog remained in a position of interfacing the digital systems with the real world. However, analog signal processing shows higher bandwidth, capable of handling far higher frequencies than their digital counter parts [1] and a capability of handling lower voltage /current signals, compared to the fixed levels of digital systems, enables

the analog VLSI to offer huge power savings, 10, 000 times [1] and an area saving by 100 times [1]. FPAA is a promising design approach for analog VLSI that provides a platform for new innovations in implementing the complex circuit applications in a small design time by the end user. For need of low design cost, testing time and design efforts, the demand for FPAA is increasing. In neural networks, signal conditioning, fuzzy controls, multi valued logic and high frequency applications FPAA proves its importance [2]. In publications of the recent past, many authors have proposed schemes for FPAA based on current mode circuit techniques, including the current feedback operational amplifier (CFOA), 2<sup>nd</sup> generation current conveyor (CCII) and the allied current conveyor devices [3-6]. In these schemes, significant considerations are given to various design issues like high frequency, low power and low voltage, small area [3-5] etc. Barrie Gilbert introduced the term current mode [7]. Among various current mode approaches current conveyor (CC) attains greater popularity for its versatility rendering it more suitable for LV and LP applications [8]. A CC simultaneously offers both low impedance and high impedance inputs along with a virtual voltage short among them [8]. It exhibits very high gain bandwidth product, improved slew rate, improved dynamic range, greater linearity, small chip area and low power consumption [8-11]. By considering the input impedance of the low impedance input node, Current controlled current conveyor (CCC) was introduced [12]. It is reported that a CCC is more flexible [13], basically analog, but extendible to digital applications [13-15]. Applications like passive comparator, regenerative comparator [14], D flip flop [14, 15], XOR/XNOR [13], CMOS clock generator etc. can be seen in literature. Current negation and current duplication is very easy to obtain in case of a CCC, leading to DOCCC, MOCCC etc. 2<sup>nd</sup> generation is generally preferred, therefore CCCII, DOCCII etc. are readily seen in literature.

In this paper we present a design of a configurable analog block (CAB) using the translinear DOCCII, realized in 16nm bulk CMOS Technology using the PTM [16] CMOS model parameters. Switching arrangement is also included in the CAB, and by appropriate selection, numerous applications based on 2<sup>nd</sup> order polynomials can be realized. However, here the results of integrator and differentiator are presented.

### CIRCUIT DISRIPTION OF DOCCII

CCII has parasitic resistance  $R_X$  at the current input node and is tunable by the biasing current  $I_B$  [13]. A DOCCII provides  $\pm$  output current signals simultaneously. The block diagram of a DOCCII is given in Fig. 1.

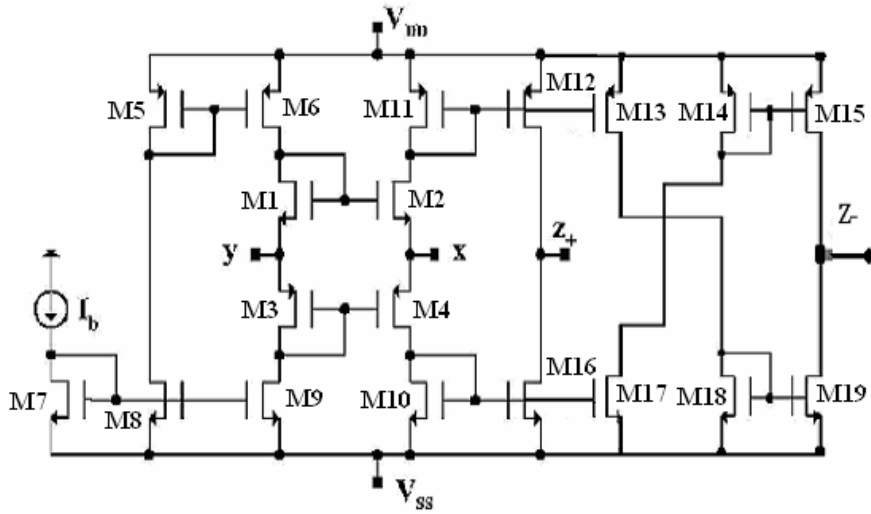


**Figure 1:** Block Diagram of DOCCII

The basic governing equation of the DOCCII is given in Eq.1.

$$\begin{bmatrix} IY \\ VX \\ IZ \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} VY \\ IX \\ VZ \end{bmatrix} \quad (1)$$

The CMOS implementation of a class AB translinear DOCCII is presented in Fig.2.

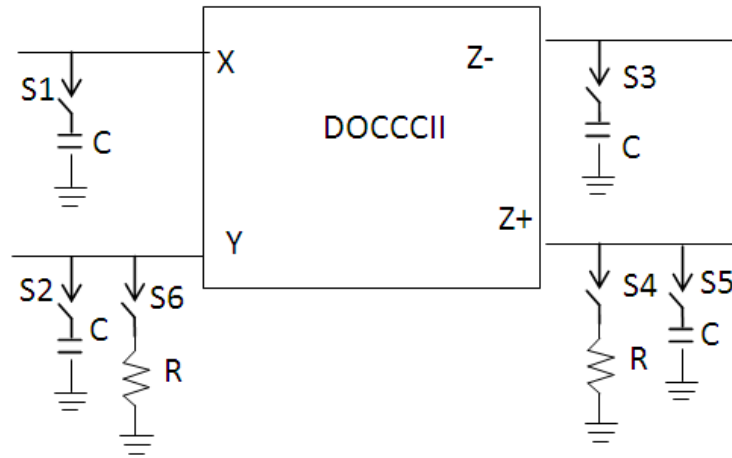


**Figure 2:** Implementation of CMOS DOCCII

### DOCCII BASED CAB

A CAB is the functional block for implementing various analog applications configurable in user domain. The CAB proposed in the present work is shown in Fig.3. The CAB is designed for implementing circuit applications which require a second order polynomial like bi-quadratic filters and oscillators. The proposed CAB contains a DOCCII, a conjoin of capacitor and resistor at node Y and at node Z+, a capacitor at node Z- and X and switches S1 – S6. In order to implement an application, switches are operated to include the required capacitors, resistors with the DOCCII. Different switching combinations can enable the realizations of a variety of applications.

The switches are no more ideal, but are a jargon of large number of non-idealities like offset voltages and currents along with parasitic resistances, inductance and capacitances. Some of them are important in consideration with FPAA scheme as their effects are dominant. Therefore a natural consideration is that their effects do not alter the circuit performance, and hence design efforts are required in this regard so that the switch dominance effects are swamped. For this purpose, an estimate is made for the total effect of various capacitances connected to a node and is assumed as a lumped model of the total capacitance at the node, e.g.  $C_{GTOTAL}$ . These estimates are usually prepared by HSPICE.



**Figure 3:** Diagram of proposed CAB

### SIMULATION RESULTS

The performance of the DOCCCI and the CAB based on it are verified by performing HSPICE simulations. The sizes of the MOSFETs used in realizing the DOCCCI of Fig.2 are presented in Table 1.

**TABLE 1:** ASPECT RATIO OF DOCCCI

Transistors	W(nm)	L(nm)
M1, M2, M7, M8, M9, M10	32	32
M16, M17, M18	32	32
M19	32	32
M3, M4, M5, M6, M11	64	32
M12, M13, M14, M15	64	32

The characteristics of the above DOCCCI are studied and the simulation results obtained are presented in Table 2.

**TABLE 2 :** CHARACTERISTICS OF DOCCCI

Current gain	1.0996
3db bandwidth	12.2825GHz
Input resistance	31K $\Omega$
Output resistance	502.05 K $\Omega$
Total power dissipation	53.25 $\mu$ watt

The output current follow-up characteristic of the DOCCII is shown in Fig.4 along with the quality of the output for a Giga hertz sine signal input is also shown in Fig.5.

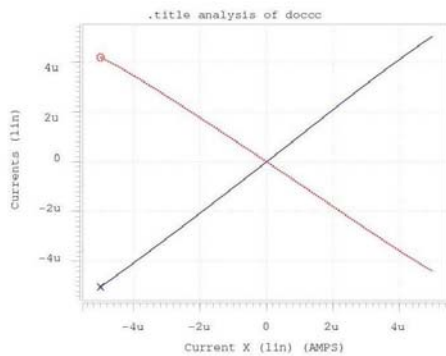


Figure 4: Output current follow up characteristics

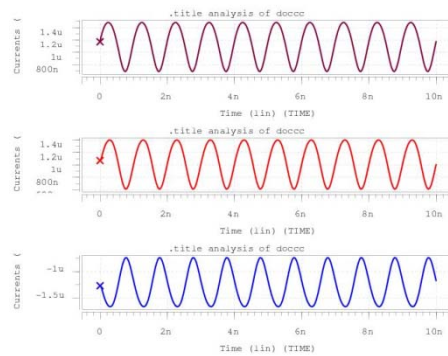


Figure 5: Output signal quality for a sinusoidal input

Furthermore, frequency response of the DOCCII is presented in Fig.6. This performance is evaluated for current input at node X.

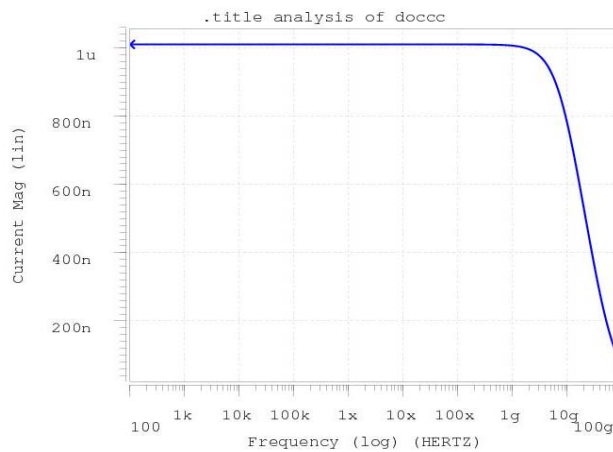


Figure6: AC Analysis of DOCCII

The working of the proposed model is demonstrated by running an application with the original circuit and then the same application is realized by using the CAB. The applications realized include integrator, differentiator from the already published work. The output wave forms are given in Fig. 7-10 and the results are summarized in Table 3.

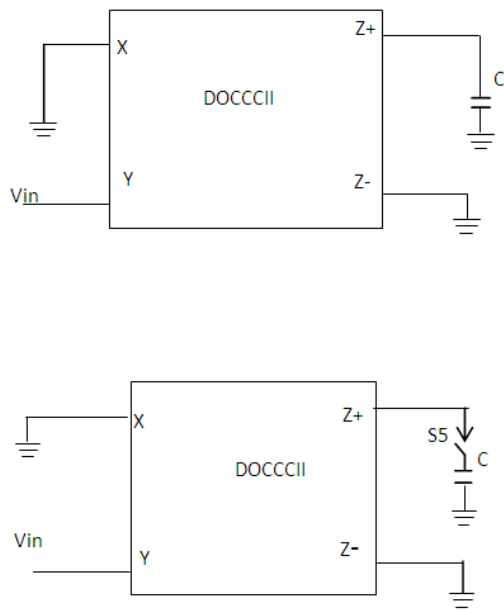


Figure 7: DOCCCI based Integrator realization using DOCCCI. (a)- Normal circuit, (b)- Integrator realization through CAB

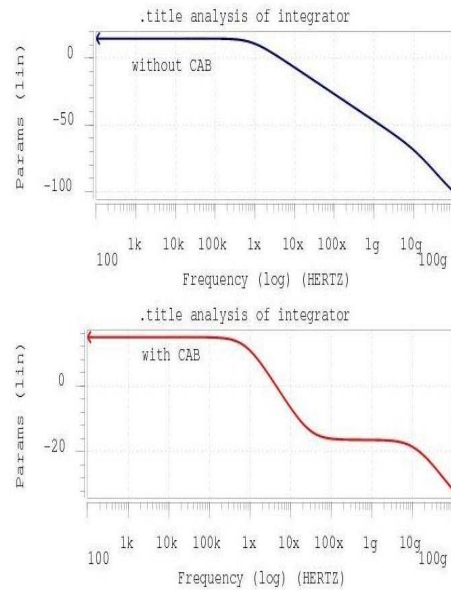


Figure 8: Performance of the Integrator realizations of Fig.7 (a) and (b).

In Fig. 7(a) an integrator structure given in [12] is realized using the proposed CAB. To include the required components on to various nodes their respective switches are closed namely (S5).

TABLE 3

Name	Without cab		With cab	
	Bandwidth	Amplitude	Bandwidth	Amplitude
Figure8	1.06907MHz	14.858 dB	1.044 MHz	14.8583dB
Figure10	19.946MHz	-31.854dB	7.906MHz	-11.0824dB

Power dissipation is same in both cases.

In Fig. 9(a) a current mode differentiator structure given [12] is realized using the CAB and the required components are included by closing switches (S1, S4).The proposed CAB can be repeated a number of times to construct an FPAA capable of realizing complex applications. The CABs will be connected by interconnect matrix on the FPAA not shown here.

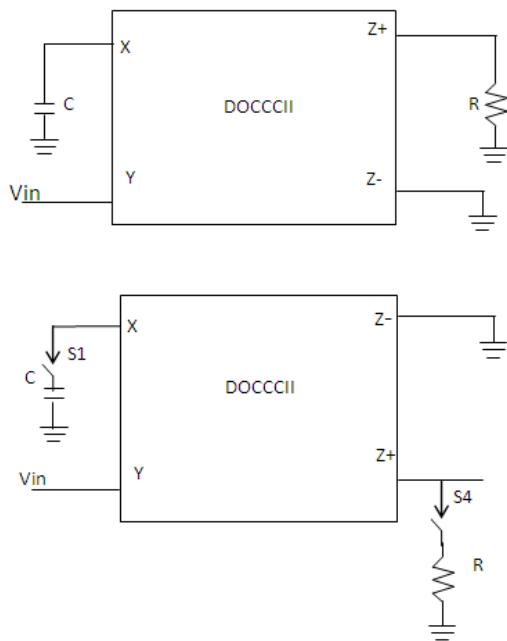


Figure 9: DOCCII based Differentiator realization using DOCCII. (a)- Normal circuit, (b)- Differentiator realization through CAB

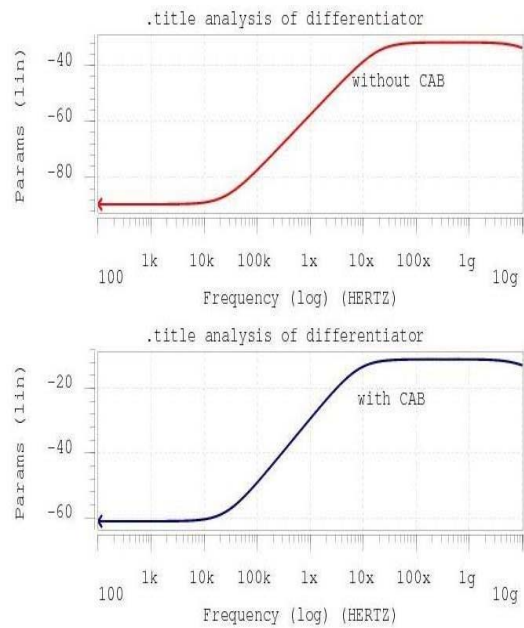


Figure 10: Performance of the Differentiator realizations of Fig.9 (a) and (b).

## Conclusion

A new design for configurable analog block based on DOCCII for high frequency applications is proposed. Using the CAB together with programmable interconnects FPAA can be constructed which will efficiently realise a number of integrators, differentiators, oscillators, filters and amplifiers.

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