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Compact Model for Dual Gate Graphene Field-Effect Transistor

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Abstract

An improvised compact model for analysis of dual gate Graphene transistor is developed which describes the current-voltage relationship of Graphene FET. The compact model presented in this paper extends to the prior models by taking into consideration the difference in the mobilities of holes and electrons in the Graphene channel which incorporates a change in carrier density and mobility in GFET. Also, the effect of top gate and bottom gate capacitances have been considered while forming the equations for Graphene channel potential which shows the effect of back gate modulation on GFET operation. The model also captures the effect of back gate modulation and gate bias dependence on the Dirac point. Parameter variation analyses is done using the developed compact model using closed form equations and the simulation results show an increase in current due to the effective mobility considered in this model and the Dirac point can be controlled using the back gate bias. The transconductance is found to be least at the Dirac point of operation due to charge neutralization.

Keywords: Dirac Voltage, Mobility, Drift velocity, Drain Current.

1. Introduction

Graphene FET has attracted a lot of attention in the recent times due to its high

potential in high speed applications. The presence of large on-state current density and transconductance of Graphene is used for high frequency applications. The short circuit current gain and cut-off frequency is quite higher when compared to the current MOS transistors [1]. The major advantage of Graphene over its contemporary semiconductors is very high carrier mobility (100,000cm^2/Vs), high saturation velocity (4-5×10^7m/s) and high current density (10^9A/cm^2) when compared to silicon. Also from the fabrication viewpoint the thin layer of Graphene makes possible ultimate vertical scaling. Graphene is one atom thick stable form of carbon which is an active research topic due to its potential. Graphene can be used only for high speed RF applications and not for digital applications due its zero band-gap. Researchers are trying to induce a bandgap in Graphene by using Graphene nano ribbons or by inducing a back gate potential which also affects the Dirac point, the voltage bias for which the conductance is minimum in GFET, so that Graphene FET can be used for digital applications.

There has been several circuit models developed [2]-[8]. One of the popular models is the compact modeling of Graphene. A compact model based on charge density model has been proposed in [2]-[4]. Compact models are the models that have a set of closed form equations and thereby can be used in the circuit simulators. Closed form equations are the set of equations that are dependent on one variable and thereby can present the characteristic behavior on changing a set of parameters. The compact models tend to neglect the device quantum capacitance when compared to the oxide capacitance, but only include the oxide capacitance leading to inaccuracies around the Dirac point.

A physics-based compact model of a long channel dual gate single layer Graphene FET (GFET) has been presented in this paper. In this paper, we utilize the intrinsic parameters of the GFET device specifically quantum capacitance, oxide capacitance, mobility and velocity saturation to derive a charge sheet model of Graphene FET (GFET) current equation. In the compact models developed so far the difference in the hole and electron mobility has not been considered [1], [2]. Here, the effect of mobility difference has been included on velocity saturation as the effective mobility and its corresponding effect on the drain current has been established. The influence of back gate on shifting of the Dirac voltage has been discussed [3]. In our work, the effect of back gate capacitance on the lateral channel voltage has been considered in forming a closed form equation for deriving the drain current in the GFET. The effect of top gate and bottom gate capacitances has been explained and has been used for derivation of channel voltage and charge neutrality point**.** The compact model characteristics are implemented using MatLab using closed form circuit equations to show the effect of voltage variation on drift velocity and carrier concentration.

II. Derivation of Compact Model

The compact model in our work derives the parametric equations for drain current considering the effect of hole and electron mobility, drift velocity, capacitance effect and surface potential.

A cross sectional view of the dual gate Graphene FET has been considered in Fig. 1. A rectangular strip consisting of bilayer Graphene is used as the device channel which is connected to drain and source contact pads. A high *k* dielectric (typically Silicon Oxide or Hafnium Oxide) slab isolates the gate electrode from the Graphene channel. The substrate is used as a back gate to induce a band gap in the Graphene FET [4].

The capacitances in FET determine the potential of the channel and the operating voltage of Dirac point. Fig. 2 shows the cross sectional view of the capacitances of Graphene FET. There are three capacitances considered in the paper C_q, C_{TOP}, and $C_{BACK.}$ The surface potential is given by the lateral voltage at the surface between oxide layer and the Graphene layer which determines the drift velocity which forms an important parameter in the development of drain current equation. A prior model for the Graphene FET model is the charge sheet density model [2], [3]. In this model the drain current is given by (1) considering the drift velocity and the carrier concentration.

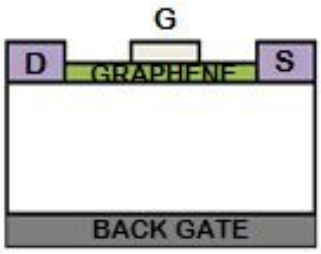

Fig.1 Cross Section of Dual Gate GFET [2]

$$I_{DS} = q\frac{W}{L}\int_0^L n(x)v_{drift}(x)dx \tag{1}$$

Where q is the charge of electron, W is the width and L is the length of the channel.

1. The New Model Equations

The above equation is modified in accordance with the following discussion. The length of the channel is bounded by $x = 0$ to $x = L$ and $n(x)$ is the carrier concentration at x. The drift velocity is dependent on the mobility of the carriers in any semiconductor device. The mobility of electrons (2100 cm^2/Vs) and the mobility of holes (1300 cm^2/Vs) differ from the approximate value of (1500 cm^2/Vs) taken in the previous works [2]-[4] and thereby a modification accommodates the effect of this mobility difference on drift velocity. The effective mobility is given in (2), where μ_h and μ_e are the low field hole and electron mobilities

$$\mu_{eff} = \sqrt{\mu_e^2 + \mu_h^2} \tag{2}$$

The drift velocity for the electrons has an inverse square root dependence on electron mobility [2], [6] and lateral electric field and is represented as (3)

$$v_{drift,e} = \frac{\mu_e V(x)}{\sqrt{1+\left(\frac{\mu_e V(x)}{v_{sat}}\right)^2}} \tag{3}$$

The drift velocity of the holes has an inverse relationship with the hole mobility and the lateral electric field [3], [6] and is given by (4)

$$v_{drift,h} = \frac{\mu_h V(x)}{1+\left(\frac{\mu_h V(x)}{v_{sat}}\right)} \tag{4}$$

Where *V(x)* is the lateral electric field in the channel, μ_h and μ_e are the low field hole and electron mobilities, and v_{sat} is the saturation voltage.

The effective drift velocity is given by (5) which is higher than the effective drift velocity considering the mobility of the charge carriers as 1500 cm^2/Vs

$$v_{drfit,eff} = \sqrt{v_{drift,h}^2 + v_{drift,e}^2} \tag{5}$$

The mobility of charge carriers is related to the phonon density. The saturation velocity is dependent on the scattering optical phonon energy of the Graphene channel on SiO_2 [3] and is given by (6)

$$v_{sat} = \frac{\Omega}{(\pi n)^{0.5}} \tag{6}$$

Where Ω is the optical phonon energy having a value of 55meV and *n* is the carrier density in the Graphene channel. The carrier density at zero gate voltage is higher than n_0 due to the charge impurities present at Graphene/dielectric interface. The carrier density $n(x)$ is modeled using the semi empirical charge voltage relationship given by (7)

$$n(x) = \sqrt{n_0^2 + (C_{TOP}(V_{TG} - V(x) - V_{TG,0}) + / e)^2} \tag{7}$$

where n_0 is the intrinsic carrier concentration, C_{TOP} is the top gate capacitance, V_{TG} is the gate bias, $V(x)$ is the voltage in the channel at *x* and $V_{TG,0}$ is the charge neutrality voltage (*i.e.*, the top gate Dirac voltage for which charge is minimum for a given back gate voltage) The modified charge neutrality voltage [3] V_o is given by (8)

$$V_0 = \frac{C_{TOP}}{C_{BACK}} V_{BG,EFF} - \gamma V_{BG,EFF}^2 \tag{8}$$

Where C_{TOP} and C_{BACK} are the top and back gate capacitances, $V_{BG,EFF} = V_{BG} - V_{BG,0}$ and γ is a fitting parameter. The lateral channel voltage [4] is given by (9)

$$V_C=\frac{C_{TOP}}{C_{TOP}+C_{BACK}+C_q}[V_{TG}-V_{TG,0}-V(x)]+\frac{C_{BACK}}{C_{TOP}+C_{BACK}+C_q}[V_{BG}-V_{BG,0}-V(x)] \quad (9)$$

Where V_{TG} is the top is gate voltage and V_{BG} is the back gate voltage and C_q is the quantum capacitance. $V_{TG,0}$ and $V_{BG,0}$ are the top gate and the back gate charge neutrality voltages.

2. Dirac Voltage

The gate bias can change the charge carriers in the channel from holes (Fermi Energy E_F<0) to electrons (Fermi Energy E_F>0) [9]. At the Dirac voltage the quantum capacitance is minimized. In this ambipolar region the electrons coming from source recombines with the holes coming from the drain.

The quantum capacitance considered in this model depends on the charge carrier concentration in the Graphene channel. The quantum capacitance has been found out using the relation

$$C_q=\sqrt{\frac{n}{\pi}}\frac{e^2}{v_f\hbar} \quad (10)$$

Where v_f is the Fermi velocity and $\hbar$ is the reduced plank constant. The Fermi velocity of the charge carriers has an inverse relationship with the quantum capacitance. As the drift velocity approaches the saturation velocity the quantum capacitance takes a minimum value. The quantum capacitance is found out to be comparable to C_{TOP} and C_{BACK}, so all the capacitance values has been considered while calculating the surface potential.

The carrier density [4] can be averaged over the channel voltage as (11)

$$\overline{n(x)}=\frac{1}{V_C}\int_{V(x=0)}^{V(x=L)}\sqrt{n_0^2+(C_{TOP}(V_{TG}-V(x)-V_{TG,0})/e)^2} \quad (11)$$

In (11) V_C is the voltage drop across the surface of the channel given by (9). The $V_{TG,0}$ is the top gate charge neutrality voltage for which the carrier concentration is minimum for a fixed back gate bias.

Together (3) to (9) forms a closed model that allows the determination of current voltage characteristics of a Graphene dual gate field effect transistor. The modifications done so far are implemented in the drain current equation. Specifically by substituting (5) and (11) in (1) the drain current is obtained as (12)

$$I_{DS}=\frac{qW}{L}\int_{V(x=0)}^{V(x=L)}\overline{n(x)}v_{drift,eff}(x)dx \quad (12)$$

The compact model has been implemented using Matlab. The channel current obtained after all the modifications is a closed form equation and thereby can be solved by variation of a parameter and the corresponding characteristics of the parameter dependence is obtained. The modulation of the channel characteristics due

to the back gate voltage can be seen as the Dirac voltage depends on the back gate bias.

3. Simulation Results

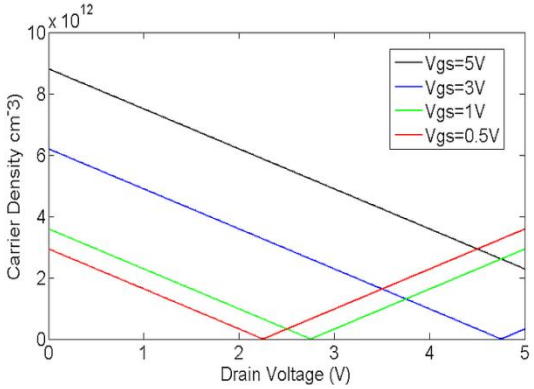

Fig. 4 Dependence of Carrier Density on Drain Voltage (Matlab simulation for (7)). The carrier density is least at the Dirac point indicating the minimum conductance which results in minimum drain current in the Graphene Channel. The back gate voltage modulates the Dirac point.

Fig. 4 shows the carrier density profile of Graphene FET. The simulation demonstrates the ambipolar nature of the Graphene FET as the carrier density first decreases then increases showing that the carrier concentration of electrons is more on the right side of Dirac voltage while holes are the majority carriers on the other side. The carrier density is least at the Dirac point due to charge neutrality; thereby the drain current is also least at the Dirac voltage. As a consequence the transconductance will be also lowest at this point. The ambipolar property Graphene FET is used for high speed device for such as RF Mixers, Oscillators [3], [4].

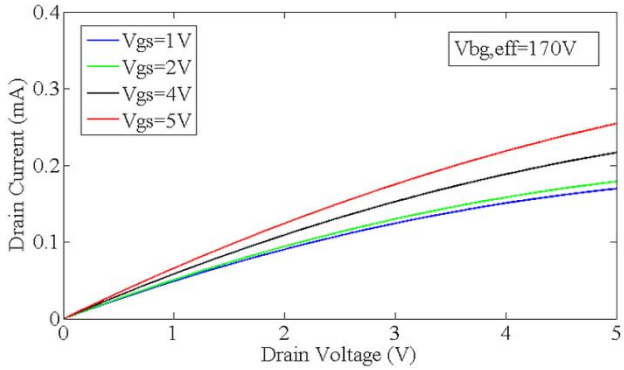

Fig 5. Current-Voltage behavior of Graphene FET (Matlab simulation for (12)). The current increases for a given drain bias when the top gate voltage is increased.

Fig. 5 demonstrates the forward characteristics of the Graphene FET, for a condition when the effective back gate bias voltage is maintained at 170V. The drain current increases with the drain bias and then saturates as the biasing voltage increases which is in accordance to the characteristic trait of a Graphene FET [3]. The drain current increases for constant drain voltage, since the carrier density increases as the top gate bias is increased.

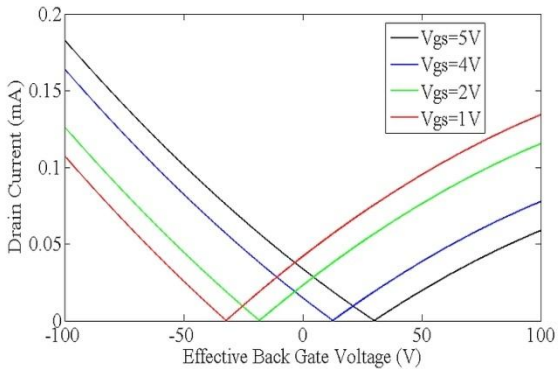

Fig.7 Dependence of drain current on the effective back gate voltage (Matlab simulation for (12)). The drain current is minimal for a particular voltage which is called as charge neutrality voltage.

Fig.7 demonstrates the dependence of drain current on the effective back gate voltage. The drain current shows a least value for a particular back gate voltage that is, a point of minimum conductance corresponding to the charge neutrality point. The back gate voltage is varied between -50V and 50V. For different top gate bias the corresponding back gate voltage for charge neutrality voltage differs which accounts for the shift in Dirac voltage due to the dual gate nature of Graphene FET.

IV. Conclusion

In this paper we have proposed a closed form compact model for dual gate Graphene FET to obtain the drain current. The model accepts the different mobilities of electrons and holes which have been used to obtain effective mobility. This effective mobility has been used in computation of drift velocity in place of average mobility which results in higher value of drift velocity at higher electric field.

The paper has incorporated the effect of top and back gate capacitances on the Graphene channel potential and charge neutrality voltage. The dependence of charge neutrality voltage on the top and back gate capacitances shows a nonlinear behavior which has been characterized by a fitting parameter. The charge neutrality voltage controls the carrier concentration and carrier density which shows the dependence of drain current on the top and back gate capacitances. The quantum capacitance contributes to the effective top gate electrostatic capacitance but it has negligible effect on the back gate capacitance.

The influence of back gate voltage on the channel current has been found out. The channel current shows a drop at the charge neutrality voltage due to charge neutralization at this point which has been correctly depicted by the dependence of drain current on effective back gate voltage. The back gate voltage modulates the channel operation by inducing a band-gap in the Graphene and thereby controls the Dirac point of operation as can be seen from Fig. 7. The transconductance is found to be least at the Dirac point of operation as the drain current is minimum due to neutralization of charge carriers.

For future model development the compact model can be implemented in circuit simulators and can be modeled using Verilog-AMS.

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