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Optimization of Zero Crossing Digital Phase- Locked Loop Performance in Carrier Synchronization System

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Abstract

This paper presents a systematic procedure for optimization of the performance of a second orderzero crossing digital phase locked loop (ZCDPLL) in carrier synchronization systems. For this purpose both the acquisition and noise performances of ZCDPLL have been extensively studied for different loop design parameters. From the studythe best compromise between the acquisition and noise performance of the loop is adopted to obtain the values of loop parameters for optimum performance.

Keywords: Acquisition, Noise performance, Optimization of DPLL performance

I. INTRODUCTION

In the field of synchronous communication, phase locked loops (PLLs) are extensively used for a long period to fulfil different purposes [1,2]. During the last few decades, implementation of PLL in thedigitaldomain has become very popular because of its several advantages over analog PLL. These includespeed, reliability and reduction of size and cost of digital systems. As such a lot of works has been published on digital phase locked loops regarding their structure, performance and application areas [3]-[7]. However, none of them presents aprocedure to optimize the performance of a second order zero crossing digital phase locked loop (ZCDPLL) in carrier synchronization systems. In [8] the statistical analysis of ZCDPLL was provided by Weinberg and Liu, and the values of loop parameters have been proposed for fastest transient response. But for those values of loop parameters the steady state noise performance of the loop is severely degraded.Some compromise between the acquisition and noise performances is thereforenecessary to obtain overall good performances in both the acquisition state and locked state. The best compromise known as optimization of loop performance is always neededto design a PLL when it is used for carrier synchronization. For this reason this paper is focused on the

optimization of a second order ZCDPLL. This type of DPLL is chosen due to the simplicity of its structure.In this paper the effect of different loop parameters on the acquisition and noise performances of the ZCDPLL is extensively studied. From this study, the values of loop design parameter have been proposed to obtain optimum performance of the loop.

The paper is organized as follows. Section II gives the mathematical model for operation of ZCDPLL in briefon application ofinput signal corrupted with additive white Gaussian Noise. In Section III, the effect of loop design parameters on the acquisition performance is systematically studied. In Section IV,an analytical expression for steady state phase error variance due to additive Gaussian noise is found out as a measure noise performance. The noise analysis presented here is simple but alternative to that presented in [8].The result is however same confirming the validity of the analysis. The effect of loop parameters on the noise performance is also investigated in this section. Section V describes the method of choosing loop parameters to obtain optimum performance of the ZCDPLL. Finally the article is concluded with Section VI.

II. MATHEMATICAL MODEL OF ZCDPLL

The block diagram of ZCDPLL to be studied is shown in Fig. 1.

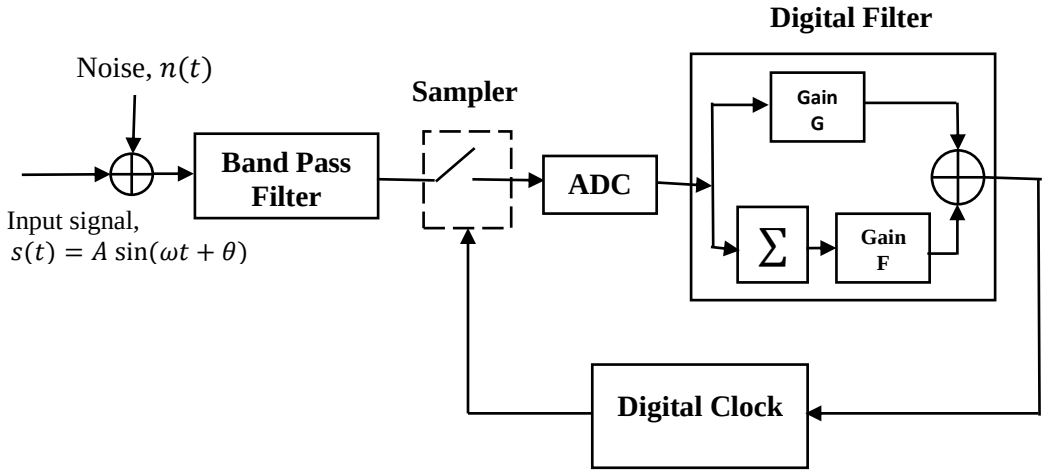

Fig. 1: Block diagram of ZCDPLL

The input signal is considered as a sinusoid of amplitude A, frequency ω (rad./s) and phaseθ rad. The perturbing noise $n(t)$is obtained by passing a stationary white Gaussian noise of constant spectral height through a band pass filter of center frequency ω having sufficiently large bandwidth. The sample values of $n(t)$obtained after a finite interval of time can therefore be regarded as independent and identically

distributed Gaussian random variable with mean zero and variance σ^2. The input to the loop can be written as

$$x(t) = A\sin(\omega t + \theta) + n(t) \quad (1)$$

The perturbed input is sampled by a digital clock of period T ($=\frac{2\pi}{\omega_0}$, ω_0 being the free running frequency in rad/s of the clock) at the positive going zero crossing instants of the input and the loop is locked on to those zero crossings. If the value of the l^{th} sample be $x(l)$ then

$$x(l) = x\big(t(l)\big) = A\sin(\omega\, t(l) + \theta) + n(l) \quad (2)$$

The sample values are passed through an A/D converter and a digital filter consisting of a gain G in parallel with another gain F and a summer. The filtered output $c(l)$is used to control the next period of the digital clock according as

$$T(l+1) = T - c(l) \quad (3)$$

Here $T(l)$ is the time interval between $l^{th}$and $(l-1)^{th}$ sampling instants. Therefore

$$T(l) = t(l) - t(l-1) \quad (4)$$

Assuming $t(0) = 0$ it follows from (3) and (4)

$$t(l) = \sum_{i=1}^{l} T(i) = l\,T - \sum_{i=0}^{l-1} c(i) \quad (5)$$

Substitution of (5) into (2) gives

$$x(l) = A\sin\Big[l\omega T - \omega\sum_{i=0}^{l-1} c(i) + \theta\Big] + n(l) = A\sin[\Phi(l)] + n(l) \quad (6)$$

Where,

$$\Phi(l) = 2\pi l\frac{\Delta\omega}{\omega_0} + \theta - \omega\sum_{i=0}^{l-1} c(i) \quad (7)$$

is the loop phase error and $\Delta\omega=\omega-\omega_0$ is the open loop frequency error.

From the construction of digital filter, control signal$c(i)$ can be written as

$$c(i) = G\,x(i) + F\sum_{j=0}^{i} x(j) \quad (8)$$

Substitution of (8) into (7) gives

$$\Phi(l) = 2\pi l\frac{\Delta\omega}{\omega_0} + \theta - \omega\Big[G\sum_{i=0}^{l-1} x(i) + F\sum_{i=0}^{l-1}\sum_{j=0}^{i} x(j)\Big] \quad (9)$$

From (9) and (6) the difference equation of Φ can be obtained as,

$$\Phi(l+1) = 2\Phi(l) - \Phi(l-1) + G_1 \sin\Phi\,(l-1) - (G_1+G_2)\sin\Phi(l) + G_1N(l-1) - (G_1+G_2)N(l) \quad (10)$$

where $G_1 = A\omega G, G_2 = A\omega F$ and $N = \frac{n}{A}$. $G_1$and G_2 are the normalized gain values of the loop and they actually represent the loop design parameters.

In the absence of noise (10) reduces to

$$\Phi(l+1) = 2\Phi(l) - \Phi(l-1) + G_1\sin\Phi\,(l-1) - (G_1+G_2)\sin\,\Phi(l) \quad (11)$$

III ACQUISITION PERFORMANCE

The acquisition performance of ZCDPLL can be determined by the settling time (time required to attain steady state within prescribed phase error limit) in face of noise free frequency step input. Taking$\frac{\Delta\omega}{\omega_0} = 0.2$ and θ=0, settling time expressed in number of clock periods N_S has been found out from (11) for different values of G_1 and G_2 with initial conditions $\Phi(0) = 0$ and $\Phi(1) = \frac{2\pi\Delta\omega}{\omega_0}$. The variation of settling time (N_S) with G_1 for different values of G_2 is shown in Fig. 2. From Fig. 2 it is observed that for a particular value of G_2 when G_1 is small (< 0.5) large number of clock cycles is needed before the phase error settles below the prescribed limit. With the increase of G_1,the settling time at first decreases and then increases.From this figure it is evident that acquisition performance can be improved by increasing the value of G_2 and also by increasing the value of G_1up to a certain limit that depends on G_2.

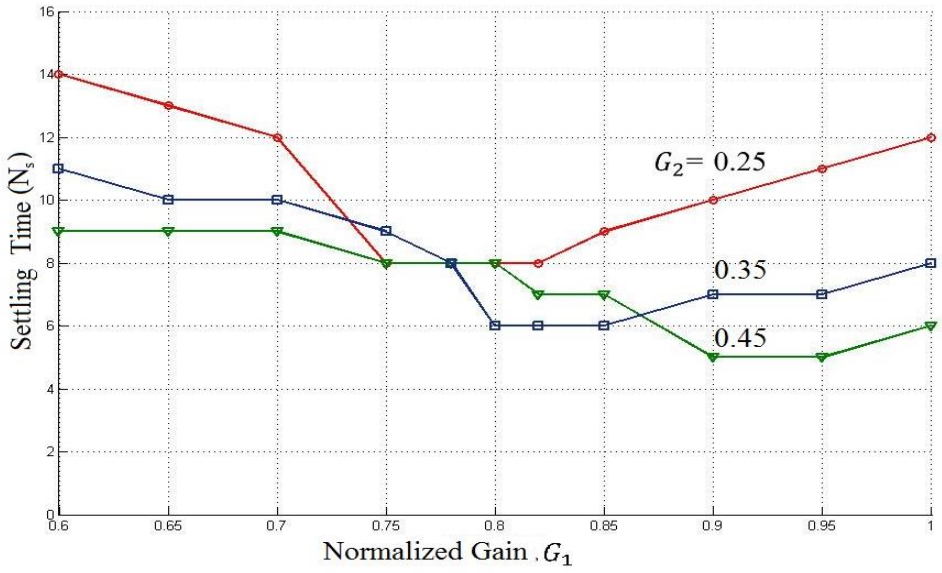

Fig.2- Variation of Settling Time with Normalized Gain (G_1) for different G_2

IV NOISE PERFORMANCE

The presence of noise with the input signal results random fluctuations of zero crossing instants of the input. As such output phase of the digital clock also fluctuates randomly. The noise performance of the loop is determined by the variance of loop phase error. The phase error or clock phase jitter is the displacement of clock phase relative to cleaned input signal phase. In the optimization procedure since we are interested in finding the effect of the loop parameters on the noise performance, sufficient information about this can be obtained from linear analysis of the loop i.e. in the case of high signal to noise power ratio (SNR). For higher values of input SNR($= \frac{A^2}{2\sigma^2} \geq 5$) the sample values of phase error Φ at each sampling instants are small and as such $sin\Phi$may be replaced by Φ. With this assumption (10) reduces to

$$\Phi(l+1) - a\Phi(l) = b\Phi(l-1) + G_1 N\,(l-1) - rG_1 N(l) \tag{12}$$

where $a = 2 - G_1 r \quad , b = G_1 - 1 \quad and\ r = 1 + \frac{G_2}{G_1}$

Inequation (12) each noise samples are statistically independent and noise sample of present instant has no co-relation with the phase error samples of present and previous instants. Therefore,

$$N(i)N(j) = \frac{\sigma^2}{A^2}\delta_{ij} \tag{13}$$

and

$$\Phi(i)N(j) = 0\ for\ i \leq j \tag{14}$$

whereδ_{ij} is the Kronecker delta function and over-bar denotes the statistical average. Remembering that $N(l)$ is a zero mean process, the mean of Φ is obtained as zero from (12). Squaring both sides of (12) and taking statistical average, following equation is easily obtained with the help of (14) and(13)

$$\overline{\Phi}^2(1 + a^2 - b^2) = G_1^2(r^2+1)\frac{\sigma^2}{A^2} - 2a\overline{\Phi(l+1)\Phi(l)} \tag{15}$$

Multiplying (12) by $\Phi(l)$ and taking statistical average

$$\overline{\Phi(l+1)\Phi(l)} = \overline{\Phi(l)\Phi(l-1)} = \frac{\left[a\overline{\Phi}^2 + G_1\overline{N(l-1)\Phi(l)}\right]}{(1-b)} \tag{16}$$

Multiplying (12) by $N(l)$ and taking statistical average

$$\overline{\Phi(l+1)N(l)} = \overline{\Phi(l)N(l-1)} = -rG_1\frac{\sigma^2}{A^2} \tag{17}$$

From(16) and (17) it is easy to obtain

$$\overline{\Phi(l+1)\Phi(l)} = \overline{\Phi(l)\Phi(l-1)} = \frac{\left[a\overline{\Phi}^2 - rG_1^2{}_1\frac{\sigma^2}{A^2}\right]}{(1-b)} \tag{18}$$

Substitution of (18) into (15) and simplification gives

$$\overline{\Phi}^2 = \sigma_\Phi^2 = \frac{B}{R} \tag{19}$$

Here $\overline{\Phi}^2$ is the mean square phase error and it is equal to the steady state phase error variance (σ_Φ^2) since Φ is a zero mean process , $R = \frac{A^2}{2\sigma^2}$ is the input SNR and

$$B = \frac{1}{2}\left[\frac{2G_1+G_2+2\frac{G_2}{G_1}}{4-(2G_1+G_2)}\right] \tag{19a}$$

Is termed as the loop bandwidth normalization with respect to the bandwidth of the band pass filter.

Taking $R = 5$, σ_Φ^2 is computed from (19) using (19a) for different values of $G_1$and G_2 and the completed variance is plotted in Fig. 3 as a function of $G_1$and G_2.

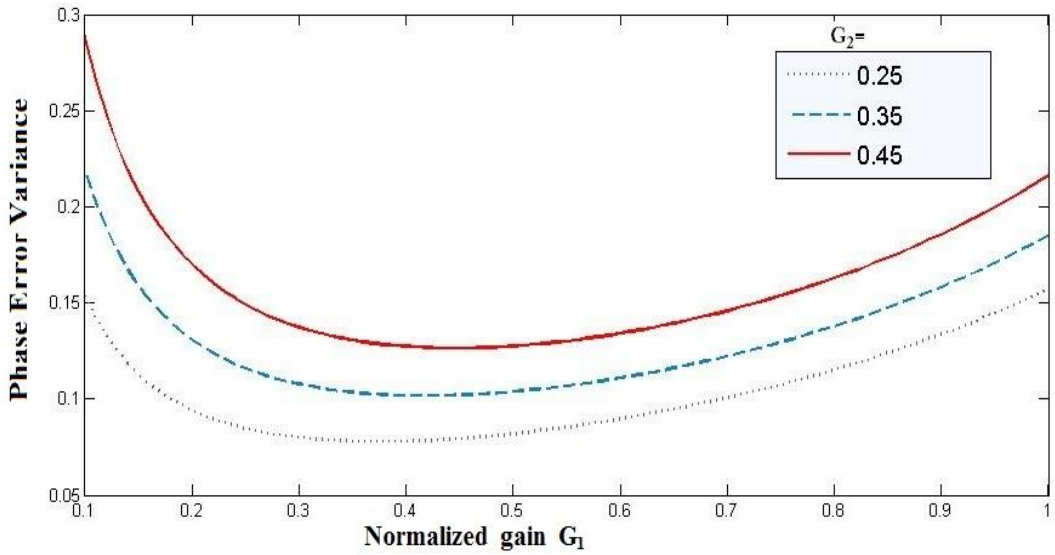

Fig.3- Plot of Phase error variance V/s Normalized gain G_1 for different G_2 ; *R=5*

V. OPTIMIZATION OF LOOP PERFORMANCE

The optimum parameters for ZCDPLL can be found out by examining the variation of settling time (N_s) and phase error variance (σ_Φ^2) with loop gain values G_1andG_2. It is observed from Fig. 2 that the settling time N_s decreases with the increase of G_2, it also decreases with increase ofG_1upto a certain value which depends on $G_2$and then increases slowly. So within the stability limit as mentioned in [7], the acquisition performance can be improved by increasing the values of G_1 and G_2upto a definite set of (G_1, G_2) . Best acquisition is obtained for the set G_1=0.95 and G_2=0.55 (only four clock cycles are needed for frequency error $\frac{\Delta\omega}{\omega_0} = 0.2$). Above these values of G_1 and G_2acquisition performance is not further improved. But the loop gain values can't be set for best acquisition because the loop phase error variance is highly increased for those gain values causing severe degradation of noise performance. From Fig. 3 it is observed that phase error variance decreases with the decrease of G_2 and for a definite G_2 it also decreases with the decrease of G_1 from its highest limiting value. It becomes minimum at $G_1 = G_1' = \sqrt{G_2} - \frac{G_2}{2}$ and then increases. So by decreasing the value of G_2 and setting $G_1 = \acute{G}_1$ noise performance can be improved. Again very low values of G_2(<0.25) and $G_1 = \acute{G}_1$ can't be chosen to obtain highly improved noise performance because in that case settling time would be large and pull out range will be shortened. For example if G_2= 0.25 and $G_1 = \acute{G}_1 = \sqrt{G_2} - \frac{G_2}{2}$pull out range $\frac{\Delta\omega}{\omega_0} = 0.194$ and the settling time for pull out range is 30 cycles. It is therefore evident that best acquisition and best noise performance can't be simultaneously obtained for a fixed set of gain values. Since it is found that improvement of one type of performance degrades the other the product of normalized loop band- width B and settling time (N_s) can be taken as the performance criterion parameter for optimization. Those gain values can be selected as optimum for which the product becomes minimum. For this purpose the values of N_s and B are computed from (12) and (17a) respectively for different values of G_1 and G_2in face ofnoise free frequency step input $\frac{\Delta\omega}{\omega_0} = 0.2$ and the computed values of N_s, B and their product are provided in table 1.

Table 1

$G_1 \rightarrow$ / $G_2 \downarrow$		**0.6**	**0.65**	**0.70**	**0.75**	**0.78**	**0.80**	**0.82**	**0.85**	**0.90**	**0.95**	**1.0**
N_s		14	13	12	**08**	08	08	08	09	10	11	12
B	0.25	0.4477	0.4733	0.50	**0.537**	0.56	0.5756	0.5923	0.62	0.668	0.7233	0.7857
$N_s.B$		6.268	6.153	6.036	**4.296**	4.48	4.6	4.74	5.57	6.68	7.957	9.43
N_s		12	11	10	09	**07**	07	07	07	08	09	10
B	0.30	0.50	0.5256	0.556	0.591	**5.614**	0.631	0.648	0.676	0.728	0.7865	0.853
$N_s.B$		6	5.782	5.56	5.32	**4.3**	4.417	4.54	4.73	5.824	7.28	8.53
N_s		11	10	10	09	08	**06**	06	06	07	07	08
B	0.35	0.554	0.58	0.611	0.647	0.67	**0.690**	0.707	0.737	0.82	0.865	0.924
$N_s.B$		6.1	5.8	6.11	5.825	5.36	**4.14**	4.242	4.42	5.74	6.055	7.39
N_s		10	09	09	09	08	08	6	6	6	6	07
B	0.40	0.611	0.637	0.67	0.706	0.738	0.75	0.77	0.8	0.858	0.924	1
$N_s.B$		6.11	5.734	6.03	6.357	5.854	6	4.6	4.8	5.148	5.54	07
N_s		09	09	09	08	08	08	07	07	05	05	06
B	0.45	0.67	0.6966	0.729	0.768	0.795	0.814	0.8344	0.867	0.928	1	1.08
$N_s.B$		6.03	6.269	6.56	6.146	6.36	6.513	5.84	6.07	4.64	5	6.48

It is observed from table 1 that the product becomes minimum for the set(G_1, G_2) = (0.8, 0.35) and this set would be selected as optimum set. However, it is to be remembered that there is no need to adjust G_1 and G_2exactly to the optimum set since the performance criterion parameter changes very slowly along the diagonal line of table 1 starting from (G_1, G_2) set(0.75,0.25) to (0.8 , 0.35). So within the above limiting range any set along the diagonal line can be selected for optimum performance of the loop.

CONCLUSION

In this paper the acquisition and noise performances of ZCDPLL in carrier tracking system are extensively studied for different loop gain values. From the whole study it is abstracted that to minimize acquisition time the loop gain values should be made larger or to minimize output phase error variance due to external noise the loop gain values should be made smaller. This result is in accordance with other types of PLL e.g. analog PLL or charge pump PLL. Considering the above effects a range of gain values has been estimated over which the acquisition and noise performances of the loop would be optimum. A small departure of loop gains along the optimum line within limiting zone as described in section V has little adverse effect on loop performance. It must be mentioned here that the optimization procedure adopted in this paper is not unique. A criteria of performance must be defined which actually depends on the loop application.

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