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Interleaved soft switched current fed full bridge DC-DC converter for Fuel cell applications

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Abstract

In this paper interleaved soft switched current-fed full bridge DC-DC converter for fuel cells to utility interface is presented. The L-C combination is used to maintain the zero voltage switching for all the switches of the converter. Soft switching allows us to operate the converter at high frequencies, reducing the size and also the cost of magnetic components becomes less. Interleaving of converters reduces the conduction losses in semiconductor devices and overall high-efficiency is maintained. Steady state analysis, design and the simulation results are presented. In the last section a comparison is made between the conventional full-bridge resonant converter and full-bridge resonant converter with voltage doubler.

Keyword- Fuel cells, high-frequency current fed dc-dc converter, interleaved converter, Zero voltage switching.

I. INTRODUCTION

Renewable energy installations are rapidly growing all around the world. Today, in the developing regions of the world where electricity is scarce, more than 1.6 billion people live without access of reliable electric power. In these areas renewable energy provides a resource that allows families to prosper and business to grow. Even though, solar and wind energy is available free of cost but very much subjected to whether conditions, therefore fuel cells are seen as potential source of energy because they provide continuous power in all seasons as long as the continuity of fuel supply is maintained. Thus, fuel cells are very important as alternative source for remote places where electrical sources are unavailable and continuous power is needed. Two important advantages of fuel cells are: (1) Do not produce polluting emissions (or) greenhouse gases. (2) Do not require supplies of foreign oil. However, these alternative energy sources cannot be used as such as they provide unregulated electric

power. Therefore, a power electronics interface is required to convert power from alternative energy sources into usable power for several applications including grid-interfacing, vehicles, residential or standalone applications.

However, the cost and durability are the major challenges to fuel cell commercialization (4000$/KW) as compared to other diesel generator (800-1500$/KW) and natural gas turbine [1]. An efficient and low cost power electronics system acts as a bridge to compensate the challenges raised with fuel cell power generation.

When fuel cell power generation is interfaced to the grid, the important stages are: (1) Front-end DC-DC converter, (2) Inverter. Of which, the front-end DC-DC converter is considered as very interesting aspect, because the efficiency of the total system depends on this stage, as it is directly interfaced with stack of fuel cells. Therefore selection of DC-DC converter topology is an important decision.

Several converter configurations are proposed [2]- [8]. Current fed converter has been justified as a suitable front-end DC-DC converter topology for fuel cells to utility interface [2]-[8] and may be a potential topology for other possible fuel cell applications. Two possible current-fed topologies for these applications are half-bridge and full-bridge.

The full-bridge and half-bridge converters are mostly used in high power applications. In both converters, the input voltage appears across the switching transistors. However, they are required to carry twice as much current in the half–bridge converter. Therefore, in high power applications, it may be advantageous to use a full bridge over a half bridge.

Efficiency, power density, reliability, and cost are important for the switched mode power supply market. The effort to obtain ever-increasing power density of switched mode power supplies has been limited by the size of passive components. Operation at higher frequencies considerably reduces the size of passive components, such as transformers and filters. In order to achieve converters with high power densities, it is usually required that they operate at higher switching frequencies, However, the high transistor switching frequencies increase the total switching loss and lower the supply efficiency. As switching frequencies increase, the switching losses associated with the turn-on and turn-off of the devices also increases.

Therefore, zero voltage or zero current switching topologies allow for high frequency switching while minimizing the switching loss. The ZVS topology operating at high frequency can improve the efficiency and reduce the size and cost of the power supply resulting in higher power densities. ZVS also reduces the stress on the semiconductor switch, which improves the converter reliability.

This paper proposes an interleaved L-C current-fed full bridge voltage doubler with parallel input and series output as shown in fig. It has the advantages of(1) Low switch VA rating (2) Low HF transformer VA rating and smaller (half) turns ratio (3) Reduced conduction losses (to half) (4) Higher efficiency (5) Lower (half) voltage rating of the rectifier diodes (6) Higher (double) frequency output ripples reducing the output filter capacitor size (7) Higher (four times) frequency input ripples reducing the input filter HF capacitor size (8) Smaller current in boost inductor reduces their size, and (9) Lower input current ripple.

Interleaving approach is useful to design higher power unit (not just two cells but may be a number of cells in parallel, also called multi-cell power conversion depends on rated output power). In some cases, the components of a power converter(s) cannot be designed for a rated output/load power. In such a case, interleaving approach is used by operating parallel converter cells. For the same load/output power, the interleaved converter has the advantages of higher input/output ripple frequency, smaller losses, higher efficiency and smaller size.

The total number of components doubles but the resulting components in inter-leaved converter is of lower ratings. For example the switches in inter-leaved converter are of lower VA rating. Switch RMS current is reduced to half, resulting in low power dissipation and smaller heat sink attached to the switches compared to single-cell converter. It reduces the total conduction losses in main and auxiliary switches, increasing the efficiency of the converter. Similarly VA rating of other components (like series inductor, parallel inductor, input inductors, rectifier diodes etc.) is also half and results in smaller volume. The frequency of input current ripple is four times of the switching frequency and of output voltage ripple is four times reducing their size. Voltage doubler is selected to reduce number of switches; the transformer turns ratio and voltage ratings of secondary side devices.

The proposed interleaved converter is of phase shift full bridge type converter. When conventional PWM converters are operated at higher frequencies, the circuit parasitic have detrimental effects on the converter performance. Switching losses are especially pronounced in high-power, high-voltage applications. To achieve ZVS, the two legs of the bridge are operated with a phase shift. This operation allows a resonant discharge of the output capacitance of the MOSFETs, and, subsequently, forces the conduction of each MOSFET's anti-parallel diode prior to the conduction of the MOSFET. It provides ZVS for the switches by using the leakage inductance of the transformer and the output capacitance of the switches. It has a somewhat higher rms current than the conventional full-bridge PWM converter, but has much lower rms currents than the resonant converters. The ZVS allows operation with much reduced switching losses and stresses, and eliminates the need for primary snubbers. It enables high switching frequency operation for improved power density and conversion efficiency. These advantages make this converter well suited for high-power, high-frequency applications. Layout of the paper is as follows:

Detailed operation and analysis during different intervals of operation of the above-mentioned converter has been presented in the section 2. All design equations required for selecting the various components of the converter are obtained from the analysis and are given. The design and performance of the two possible topologies for the present application has been compared. Results obtained from the PSIM simulation are given in Section 4.

II. ANALYSIS AND OPERATION OF INTERLEAVED CURRENT-FED FULLBRIDGE CONVERTER

In this Section, steady-state operation and analysis with ZCS concept has been explained. Before turning-off of a diagonal switch pair (S1-S4, S2-S3, S5-S8 or S6-

S7) at primary side, the other pair of primary side switches is turned on. To understand the operation and analysis, the following assumptions are made: a) Boost inductors L1andL2 are large enough to maintain constant current through them. Output capacitors are large enough to maintain constant voltage across them. b) All components are assumed ideal. c) Series inductors Llk1 and Llk2include the leakage inductances of the HF transformers. d) Magnetizing inductances of the transformers are large.

The steady-state operating waveforms are shown in Fig. The primary switches pairs S1-S4 and S2-S3in Cell 1 are operated with identical gating signals phase shifted with each other by 180^0 and the duty cycle should be kept more than 50%. The same for the switches pairs S5-S8 and S6-S7in Cell 2. The phase difference between gating signals of switches pairs S1-S4 andS5-S8 is 90^0. The operation of the converter during different intervals in a one quarter cycle is explained with the help of equivalent circuits shown in Fig. For the rest of the HF cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle.

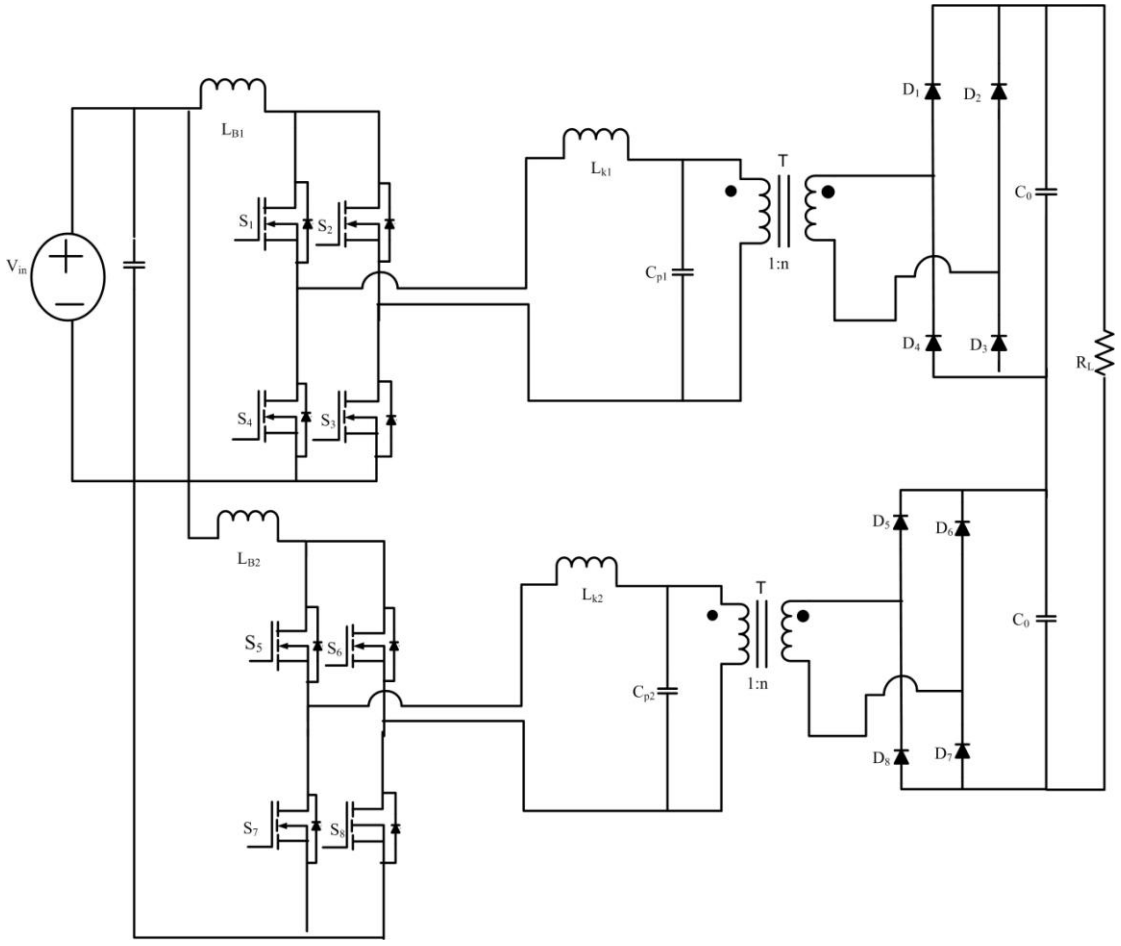


Fig 1. Interleaved current-fed full bridge converter

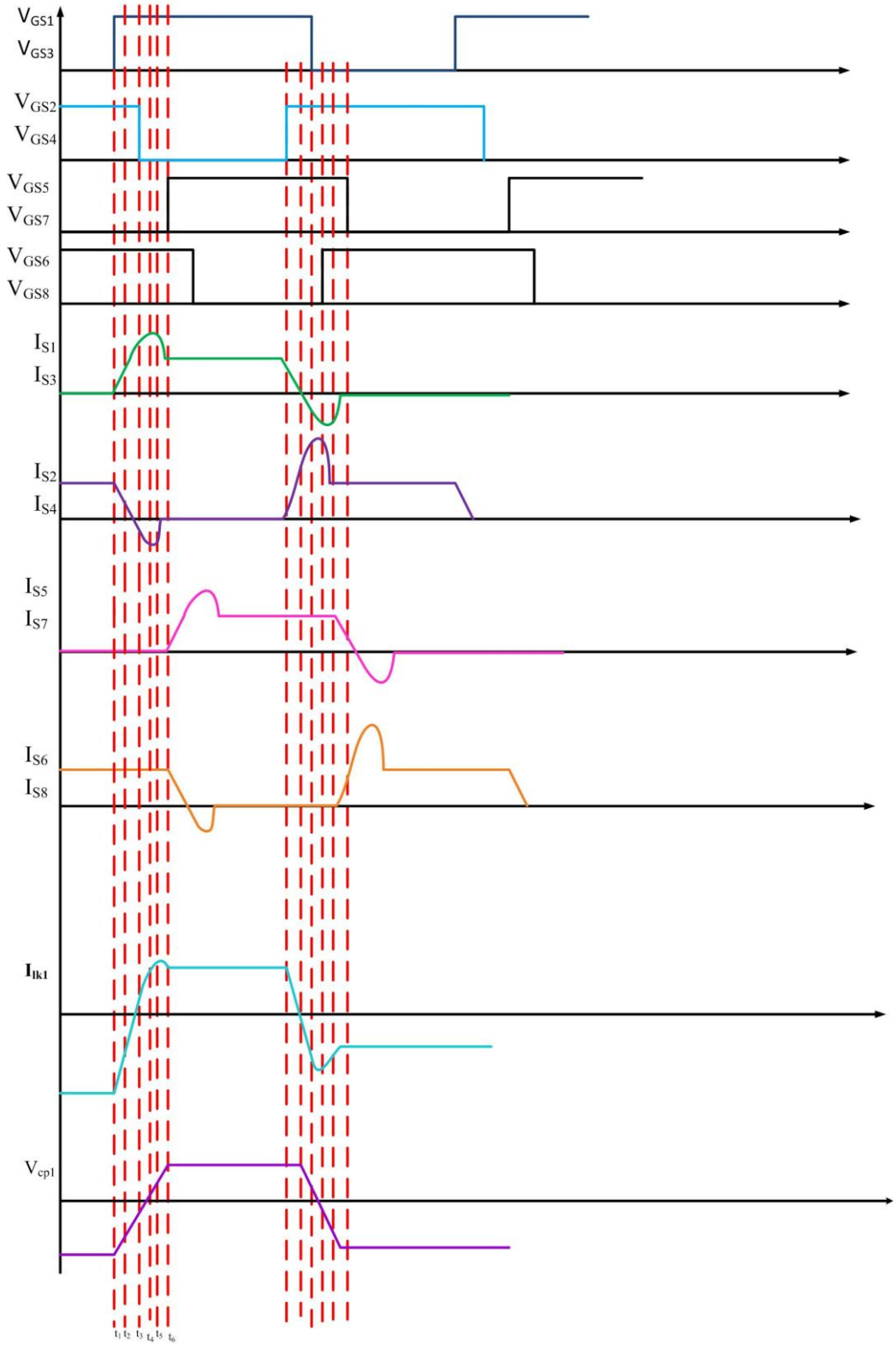


Fig: 2 Waveforms of current-fed full bridge interleaved topology

Interval 1 (Fig:3, a, $t_1<t<t_2$):

CELL 1: In, these interval primary switches S_1 and S_3 are turned on prior to S_2 and S_4. So all four primary switches of CELL-1 are conducting. Energy stored in the inductor L_k is transferred to output load. In the secondary side diodes D_2 and D_4 are in conduction state.

CELL 2: In, these interval primary switches S_2 and S_4 are conducting. The power is transferred to the output load. In the secondary section diodes D_5 and D_7 are conducting.

$I_{LK}=\frac{V}{n}[t-t_1]-I_{LB}$ **(1)**

$I_{s1}(t)=\frac{1}{2}[I_{LB}+I_{LK}]=I_{s3}(t)$ **(2)**

$I_{s2}(t)=\frac{1}{2}[I_{LB}-I_{LK}]=I_{s4}(t)$ **(3)**

Capacitor voltage is given as

$V_{cp}=\frac{-V0}{n}$ **(4)**

Interval 2 (Fig:3, b, $t_2<t<t_3$):

CELL 1: In, this interval all four primary switches are conducting. The inductor current $I_{LK}=0$ and secondary devices D_2 and D_4 are turned off under ZCS. Resonance occurs between L_k and C_p. The current through S_2 and S_4 is decreasing and becomes zero at $t=t_2$. At t_2 switches S_2, S_4 are turned off.

CELL 2: Interval 2 stays the same with interval 1.

$$I_{LK}=\frac{V_0}{nZ_r}\sin[w_r(t-t_2)] \quad \textbf{(5)}$$

$$w_r=\frac{1}{\sqrt{L_sC_p}} \quad \textbf{(6)}$$

$$Z_r=\sqrt{\frac{L_s}{C_p}} \quad \textbf{(7)}$$

$$w_r(t_3-t_2)=\sin^{-1}[\frac{nI_{LB}Z_r}{V_0}] \quad \textbf{(8)}$$

$$V_{CP}=\frac{-V_0}{n}\cos(w_r(t-t_2)) \quad \textbf{(9)}$$

Interval 3 (Fig:3, b, $t_3<t<t_4$):

CELL 1: In this interval S_1 and S_3 are conducting along with the body diodes of S_2 and S_4. The inductor current reaches the maximum value of I_p and V_{cp} is equal to zero.

CELL 2: Interval 2 stays the same with interval 1.

$$I_p=|I_{LK}(t)|_{\max}=\frac{V_0}{nZ_r} \quad \textbf{(10)}$$

Interval 4 (Fig:3, d, $t_4<t<t_5$):

CELL 1: In this interval, switches S_1 and S_3 and body diodes of S_2 and S_4 are on. The inductor leakage current i_{LK} reaches I_{LB} at $t=t_5$ and at that point, period of resonance is

terminated. That duration t_5 to t_2 is calculated by the following equation

$$\omega_r(t_5 - t_2) = sin^{-1}(\frac{nI_{LB}Z_r}{V_0})\ (\frac{\pi}{2} < \omega_r(t_5 - t_2) < \pi \quad \textbf{(11)}$$

$$\omega_r(t_5 - t_2) + \omega_r(t_3 - t_2) = \pi \quad \textbf{(12)}$$

CELL 2: Interval 2 stays the same with interval 1.

Interval 5 (Fig: 3, e, t_4<t<t_5):

CELL 1: In this interval, switches S1, S3 are on. The resonant capacitor is charged by I_{LB} which is the inductor leakage current. Diodes D_1 and D_3 starts conduction when t=t_6 and voltage of the capacitor V_{cp} becomes V_0/n. This duration is from t_6 to t_5. It is calculated by the following equation

$$(t_6 - t_5) = \frac{V_0(1+cos(\omega_r(t_5-t_2)))C_P}{nI_{LB}} \quad \textbf{(13)}$$

The output current i_0 is zero. The inductor current and voltage across the capacitor is given by the following equations

$$i_{LK}(t) = I_{LB} \quad \textbf{(14)}$$

$$V_{cp}(t) = -\frac{V_0}{n}cos(\omega_r(t_5 - t_2)) + \frac{I_{LB}}{C_P}\ (t - t_5) \quad \textbf{(15)}$$

The currents through the switches is given by

$$i_{S1}(t) = i_{S3}(t) = I_{LB} \quad \textbf{(16)}$$

$$i_{S2}(t) = i_{S4}(t) = 0 \quad \textbf{(17)}$$

CELL 2: Interval 2 stays the same with interval 1.

Interval 6 (Fig: 3, f, t_5<t<t_6):

CELL 1: In this interval, S_1, S2, D1, D3 are on. The Cp is charged by the input inductor and the voltage of the capacitor is equal to V_0/n. The following equations show capacitor voltage V_{cp} and output current i_0.

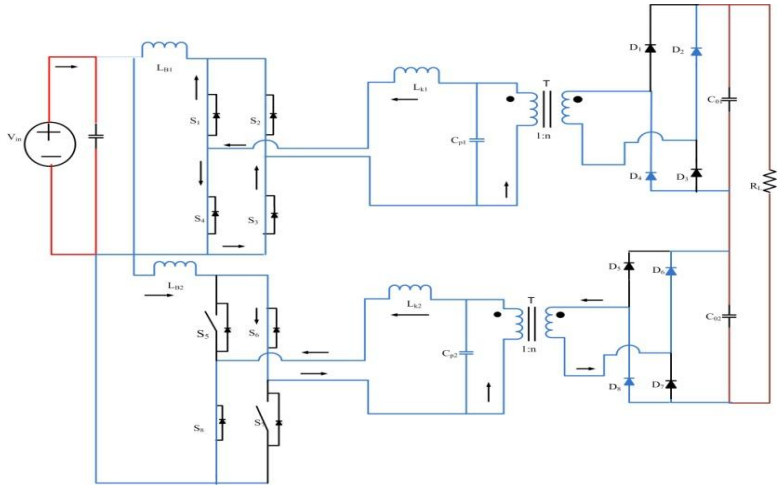
$$V_{cp}(t) = \frac{V_0}{n} \quad \textbf{(18)}$$

$$i_0(t) = \frac{1}{n}I_{LB} \quad \textbf{(19)}$$

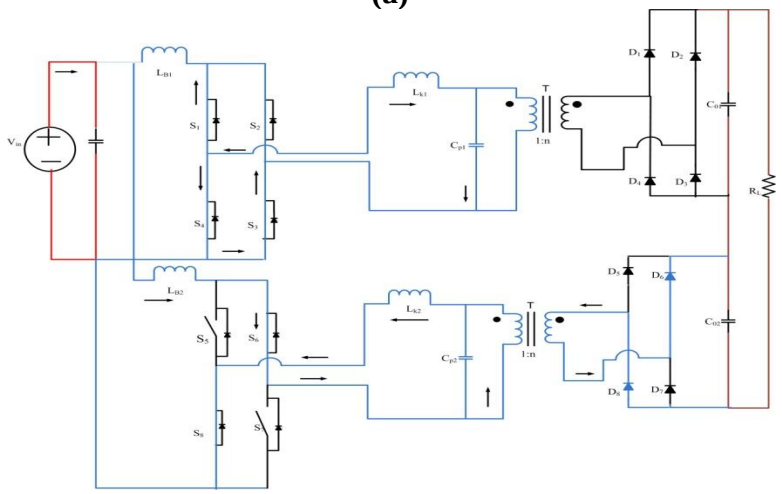
The total switching period is T_s. Therefore, T_s/2 will be the duration from mode 1 to mode 6. It is given by the following equation

$$\frac{T_s}{2} = (t_2 - t_1) + (t_5 - t_2) + (t_6 - t_5) + (t_7 - t_6) \quad \textbf{(20)}$$

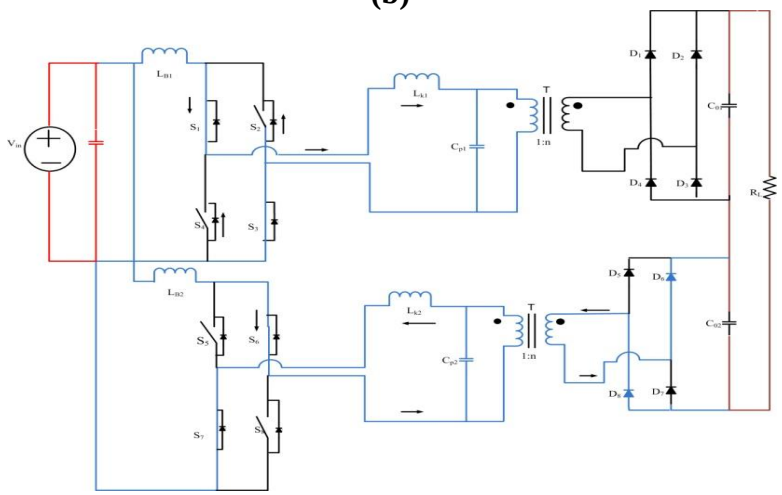
CELL 2: Interval 2 stays the same with interval 1.



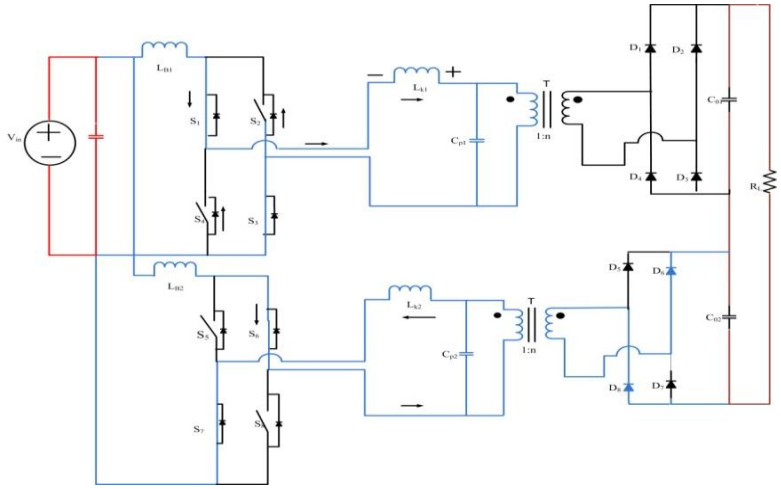
(a)



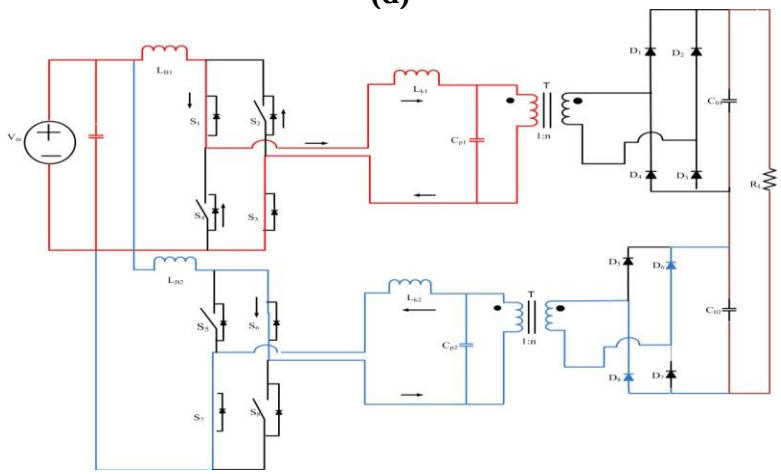
(b)



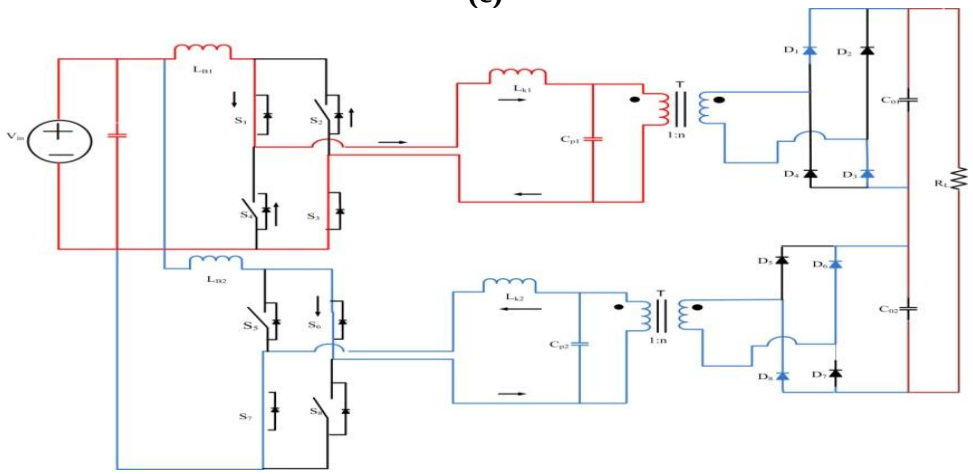
(c)



(d)



(e)



(f)

Fig 3. Equivalent circuits during different intervals of operation of the proposed converter for the waveforms shown in Fig. 3

V. SIMULATION RESULTS

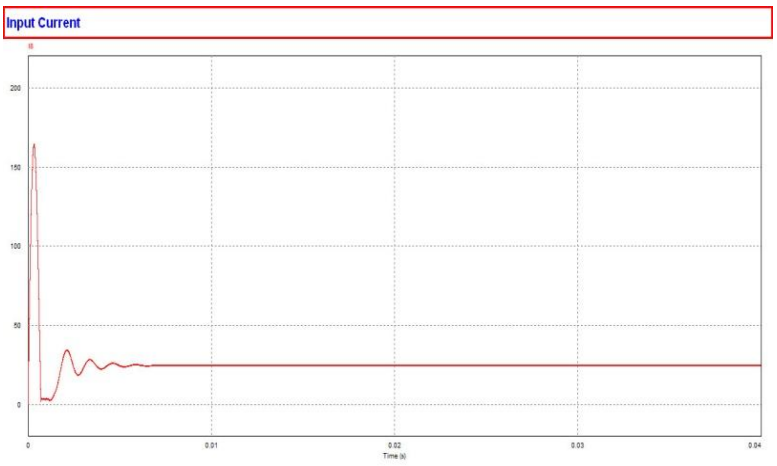
TABLE I

Parameter	Interleaved current-fed full bridge converter	Interleaved current-fed full bridge with voltage doubler
Switch current	12.066	7.34
Switch voltage	44.6	44.5
Input current	24.66	14.85
Output current	2.244	1.2127
Output voltage	359	388
Transformer turns ratio	1:4	1:2
Efficiency	90.72	93.93

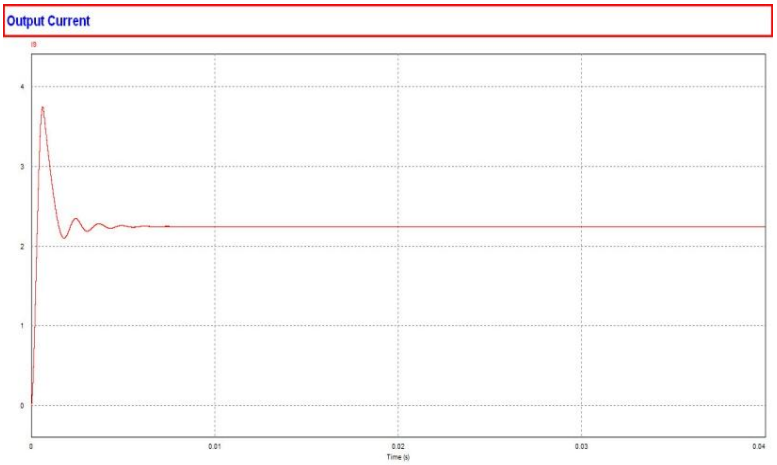
It is clear from investigation that interleaved Full bridge converter presents higher efficiency and requires smaller heat sink (due to reduced conduction losses). Soft-switching for wide operating range permits higher switching frequency operation resulting in smaller, low cost and light weight magnetic components. Phase-shift modulation results in less input current ripples at fuel cell.

In the fig4, a and b represents the input current and output current while c is with respective to output voltage. Soft switching is shown in d where the current is current is reaching zero and then the voltage is increasing. The transformer primary and secondary voltages are shown in e and f.

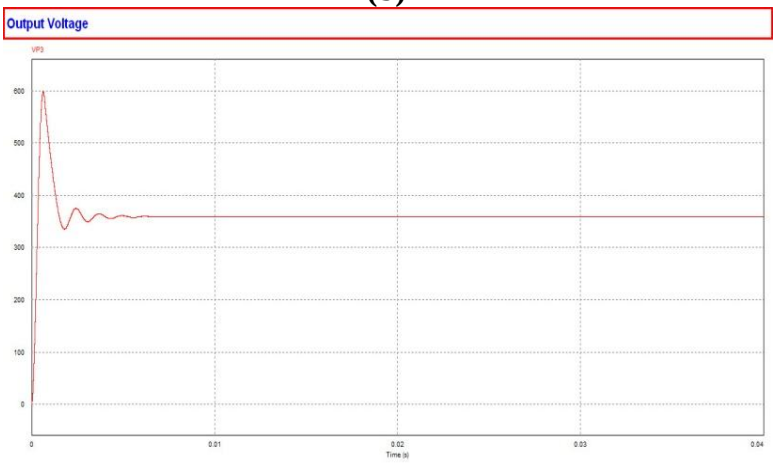
In fig 6 (a) and (b) represents the output voltage and output current of interleaved current-fed full bridge converter with voltage doubler. The soft switching is shown in (c) where the voltage starts raising at the point where the current becomes zero. The transformer primary and secondary voltages of cell 1is represented in (d). At last the inductor current waveform is with respective to (e).



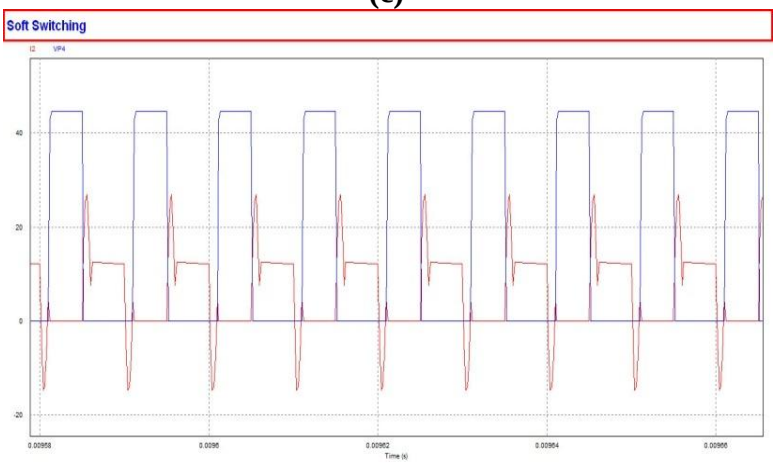
(a)


Output Current
Time (s)

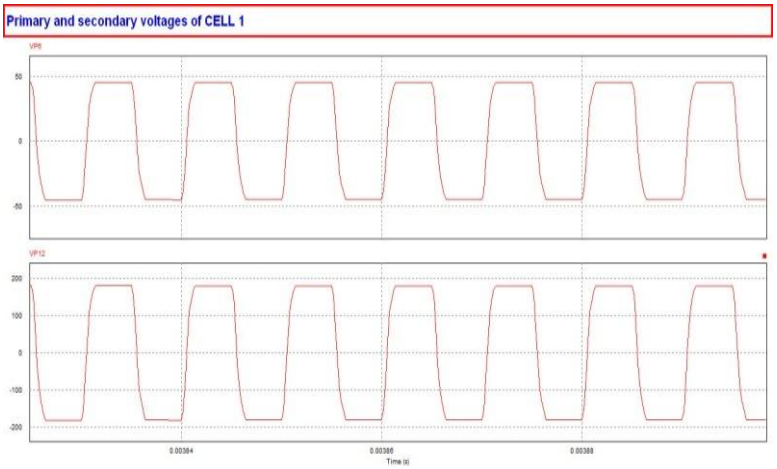
(b)


Output Voltage
Time (s)

(c)


Soft Switching
Time (s)

(d)



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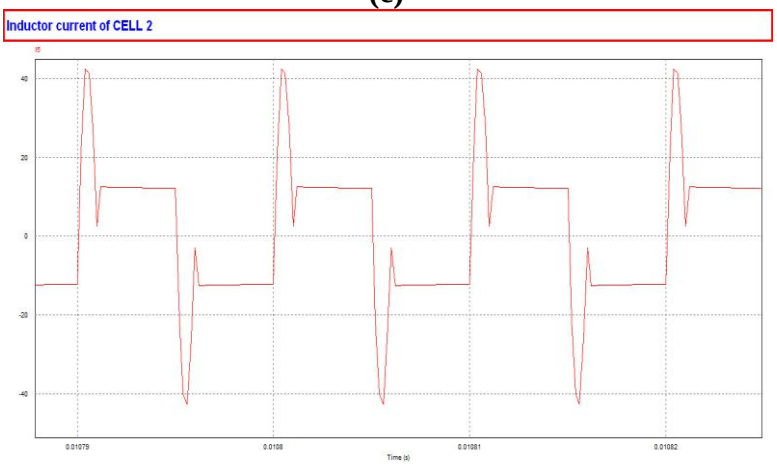


(f)

Fig 4. Simulation Waveforms of Interleaved topology

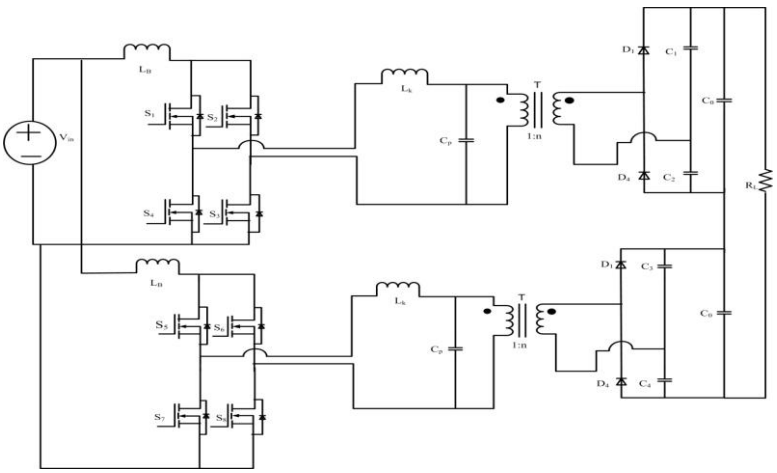
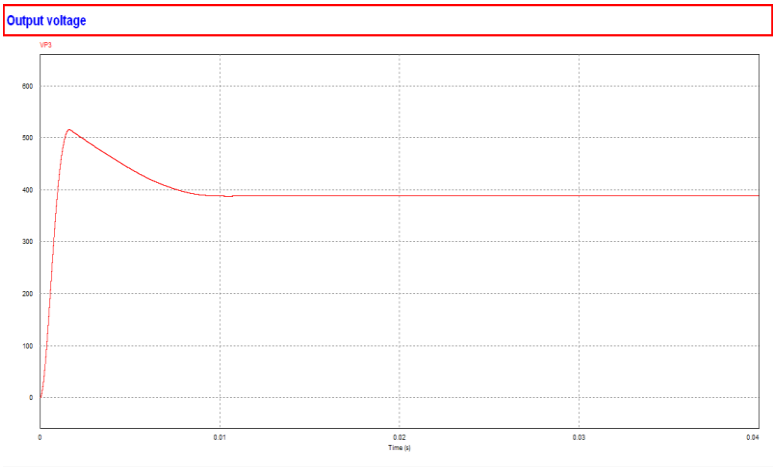
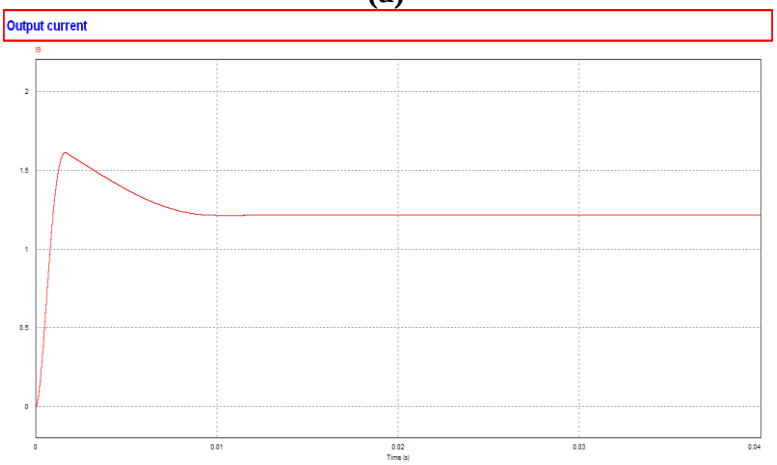


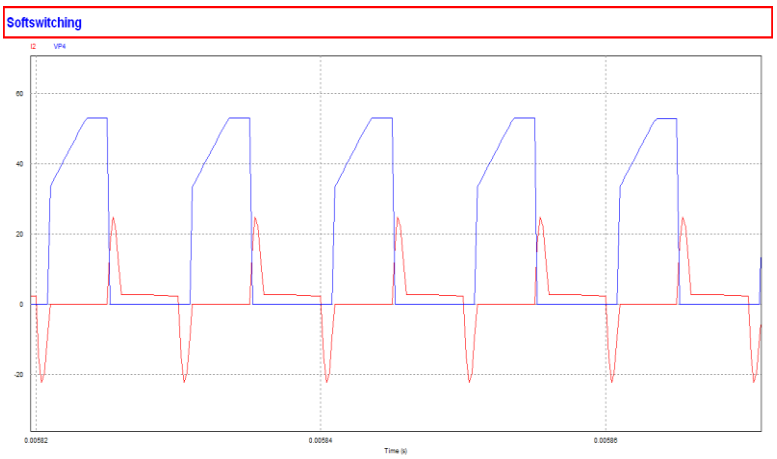
Fig 5. Interleaved current-fed full bridge converter with voltage doubler


Output voltage
VP3
600
500
400
300
200
100
0
0
0.01
0.02
0.03
0.04
Time (s)

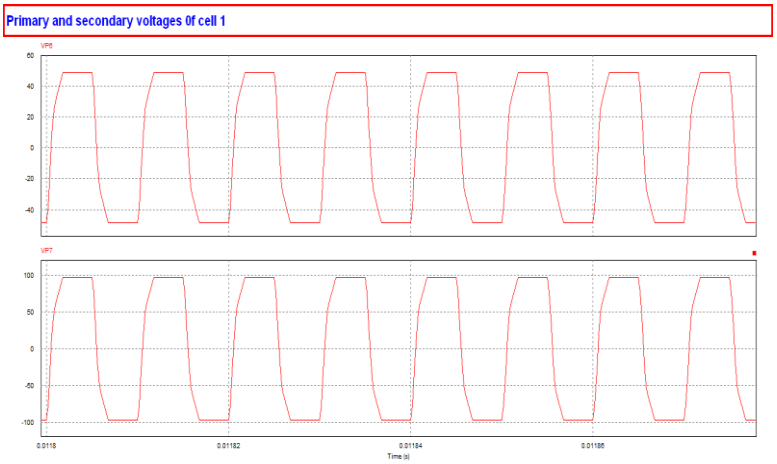
(a)


Output current
I3
2
1.5
1
0.5
0
0
0.01
0.02
0.03
0.04
Time (s)

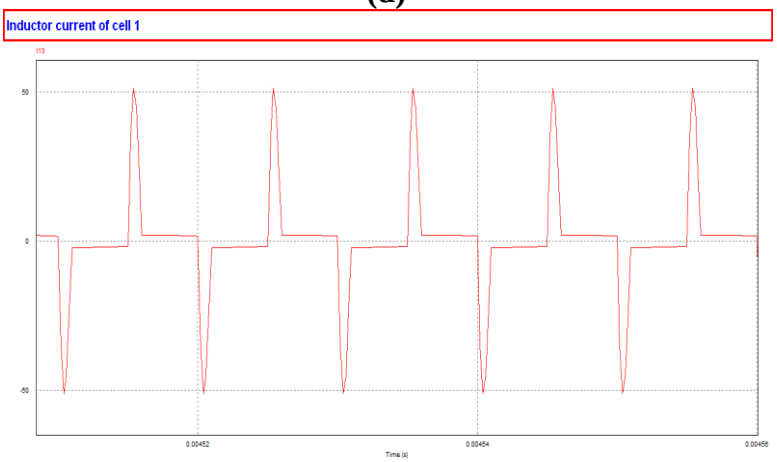
(b)


Softswitching
I2
VP4
60
40
20
0
-20
0.00582
0.00584
0.00586
Time (s)

(c)



(d)



(e)

Fig 6. Simulation waveforms of interleaved topology with voltage doubler

VIII. CONCLUSION

In this paper, soft switching is obtained for current fed full bridge DC-DC converter which is apt for fuel cell applications. It can be operated at high frequencies because of soft switching. Efficiency of 94% is obtained at fu load power of 400w. Because of current sharing, reduction in transformer turns ratio, efficiency can be further increased to if inter-leaved concept is used. Efficiency still increases by using voltage doubler. Therefore, this type of converter is suitable for fuel cell applications because of reduction in cost, weight, high efficiency, etc.,.

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