International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 10 (2015) pp. 26221-26229

http://www.ripublication.com

Power Optimization of Feed Back Shift-Register for LBIST

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Abstract

The main research aspects of VLSI are testing, low power heuristics and providing security from malicious attacks. So, here efficient scrutiny equipment named as LBIST is used to find stuck-at faults and malicious effects. We present a low power testable approach for Feedback Shift Register (FSR). Here, the FSR is designed using testable reversible sequential logic primitive. By replacing the flip-flop with testable Reversible logic gate named as FREKIN gate we can achieve low power requirement. The importance of the proposed work lies in the fact that it provides the design of reversible sequential circuits completely testable for any stuck-at fault by only two test vectors and thereby eliminating the need for any type of scan-path access to internal memory cells and also diminishes power. The design is targeted for SPARTAN 3E FPGA.

Keywords: LBIST, FSR, REVERSIBLE LOGIC, Fredkin Gate, TPG, Verilog.

I. INTRODUCTION

The main challenging areas in VLSI are cost, testing, performance, area, reliability and power consumption. The demand for portable computing devices and communication systems is in rapid increase nowadays. These applications require low power dissipation for VLSI circuits. The ability to design, fabricate and test Application Specific Integrated Circuits (ASICs) as well as FPGAs with gate count of the order of a few tens of millions has led to the development of complex system on chip. The hardware components in a SOC may include one or more memories,

processors and dedicated components for accelerating critical tasks and interfaces to various peripherals.

Testing of integrated circuits [1] (ICs) is important to ensure a high level of quality in product functionality in both commercially and privately produced products. In the modern System-on-Chip (SOC) design many cores are integrated into a single chip. Some of them are embedded and outside of the chip cannot be accessed. Such SoC designs make the test of these embedded cores become a great challenge. Built-In-Self-Test (BIST) is one of the most popular test solutions to test not only stuck-at faults but also malicious Trojans [2] which are in built in the circuit. In Automatic Test Equipments (ATE) is the growing disparity between the external bandwidth (ATE speed) and the internal one (internal frequency of the circuit under test) and as the importance of delay faults is increasing with newer technologies and the cost of test pattern generation as well as the volume of test data keeps increasing with circuit size, so an alternative solution is needed. Built-in self-test refers to techniques and circuit configurations that enable a chip to test it-self. In this methodology, test patterns are generated and test responses are analyzed on-chip.

Here, the other aspect is power dissipation. As in conventional circuits the node voltage levels are switched from ground voltage to supply voltage. The energy it needs is KTln2 [3] so, power dissipation is increases. In order to reduce this wasted power need to reduce voltage transitions or eliminate these transitions. The ultimate solution [4] to diminish the power dissipation is reversible logic circuits which is using conservative logic. By having these logic gates we can reduce power dissipation.

This paper describes a new method proposed for power optimized LBIST for a Feed-Back-Shift register. The presented FSR have been implemented by using Reversible logic gate called Fredkin Gate. Here the Test Pattern Generator (TPG) and Test Response Analyzer (TRA) are used in the LBIST architecture without using MISR logic to compact the output response.

II. PREVIOUS WORK

Logic Built-In-Self-Test (LBIST) uses a Pseudo-Random Pattern Generator (PRPG) to generate pseudo-random test patterns that are applied to the circuit under test and an output response compactor for obtaining the compacted responses to these patterns, called signature as shown in figure 1. An incorrect signature indicates a fault.

The LBIST controller contains circuitry that controls the testing process: generation of pseudo-random test patterns, their application to the circuit under test and compaction of output responses. The controller first initializes the PRPG to a given initial state and then counts the required number of test patterns. The initial state and the number of test patterns are defined by the test initialization parameters.

Pseudo-random patterns generated by the PRPG are fed into a circuit under test and propagated through its modules. The resulting output signals are provided to the output response compactor, typically implemented by a Multiple Input Signature Register. The MISR computes a signature representing the cumulative value of the output responses and forwards it to the decision logic.

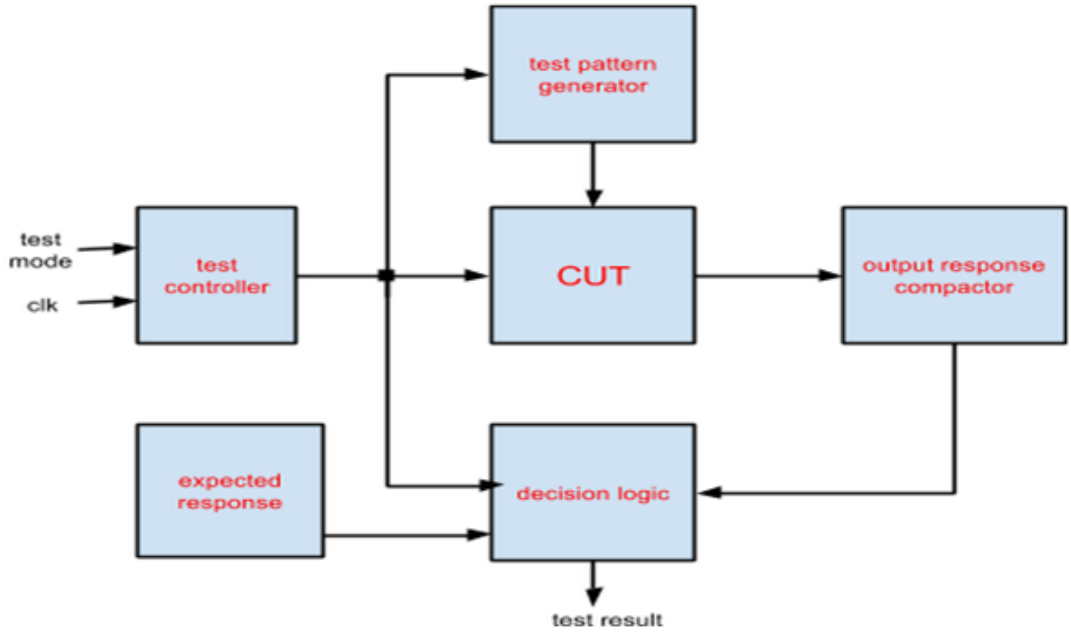

Figure 1: Traditional LBIST

Since the output responses are compacted and a faulty circuit can produce the same signature as a fault-free one.

Decision logic compares the signature computed by the MISR to the expected "good" signature. Then if the MISR signature matches the expected signature, then the circuit passes the test. If not Circuit fails the test.

The test initialization parameters and expected signature are typically stored in a memory (e.g. Flash) or hard-wired into a chip during the manufacturing stage.

The management of the traditional LBIST is performed using a processor which either resides on a chip, or on the same board as a chip. The processor initiates LBIST by sending a "test mode" signal to the LBIST controller. Typically, LBIST is initiated at power-up and/or restart, or in response to some external trigger, e.g., if a hardware or software supervising the chip indicates a fault.

III. PROPOSED WORK

In a traditional LBIST the test patterns are generated by TPG and applied to the circuit which is under test and the output obtained by the circuit is compacted into MSIR to generate the signature. And if the signature is not correct then this test is decided as a faulty. But in the proposed LBIST the output is not captured into MISR instead the operation is done inside the TOC block it-self.

The operation of the proposed design is shown in the figure 2. The FSR is designed by using flip-flops and multiplexers. To optimize the power flip-flops have been designed by testable reversible logic gates. By using this reversible operation the

power consumption can be reduced. The efficient LBIST [5] architecture contains different types of components such as state enabler, Test input Generator (TIG), Feed Back Shift Register (FSR) and Test output checker (TOC). The TIG is used to generate the test patterns which are required to test the FSR module. State enabler block will generate the control signal to the FSR, when it should take test inputs and when it should take functional inputs. So here the control signals are the selection inputs for the multiplexer which decides the FSR input connections. The multiplexer has two inputs among those one is test input generated from TIG block and another one is the functional input which is the feedback function of the previous flip-flop.

The obtained output from the FSR is connected to the De-mux which gives two outputs. As shown in the figure 3. The De-Mux output is connected to the input of TOC component. Where inside the TOC, expected patterns are generated which are XORed with the input patterns applied to the TOC. And the output of these XOR gate is given as a input for the OR gate to check whether there are any faults present in this or not. If the output obtained from the OR gate is zero then the circuit is called as a Fault free. If it is 1 then the circuit is Faulty circuit.

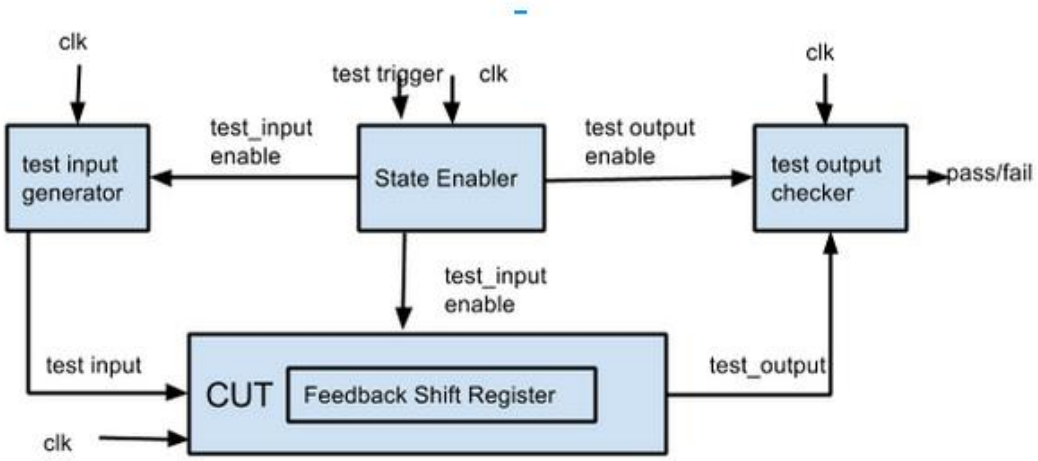

Figure 2: Efficient LBIST architecture

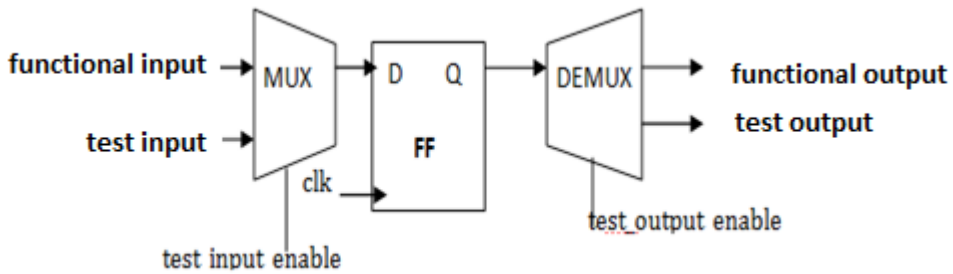

Figure 3: Flip-flop Design for FSR

As shown in figure.3 the Test input enable and test output enable signals are used to control the mux and demux operations. If the test input enable signal is high

then test input is connected as an output of mux to the input of flip-flop, if the test input enable is low then the functional input is connected as a input to the flip-flop. And similarly the test output enable is high then flip flop output is connected to the Test output and if it is low then flip-flop output is connected to the functional output. In this design the test patterns required to test the FSR logic are given in below table 1. First the FSR is tested by applying all 8bit 0's and 1's as a first test patterns.

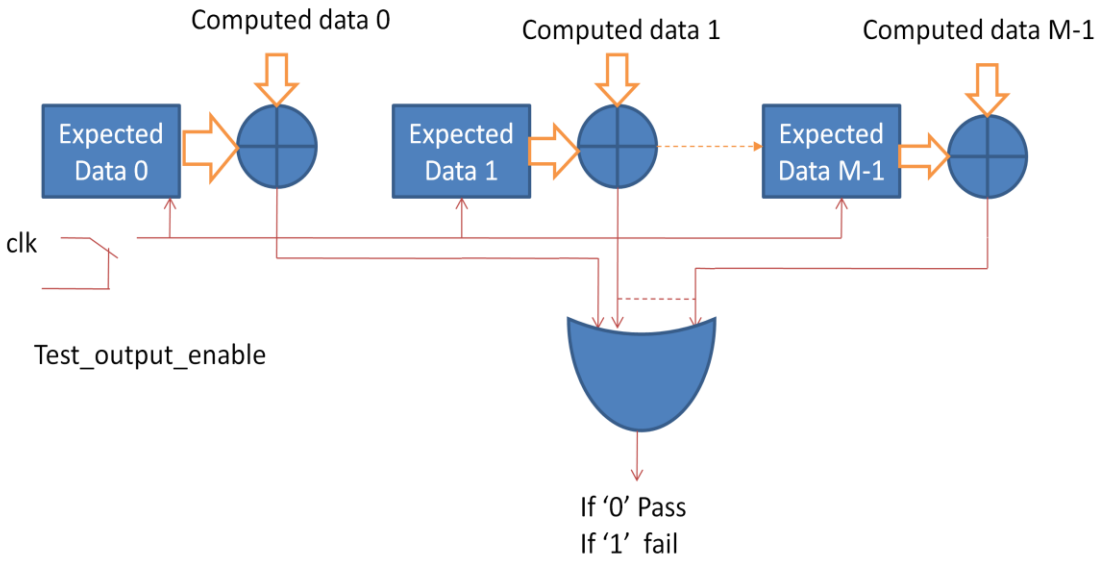

Figure 4: Architecture of TOC

As shown in figure.3 the flip-flop used in FSR design is implemented by Reversible logic gates. The flip-flop is designed by using Fredkin gates as shown in figure.5. It is designed as Master Slave flip-flop with two control inputs which are used for testing logic for any stuck-at-fault errors in a design. The Fredkin gate is a popularly used reversible conservative logic gate[6], was first proposed by Fredkin and Toffoli. The Fredkin gate [7] shown in Figure.5 can be described as a mapping inputs (A, B, C) to outputs (P = A; Q = A_B + AC; R = AB + A_C); where inputs are A, B, C and outputs are P, Q, R. By using reversible logic fredkin gate D latch[8] was implemented.

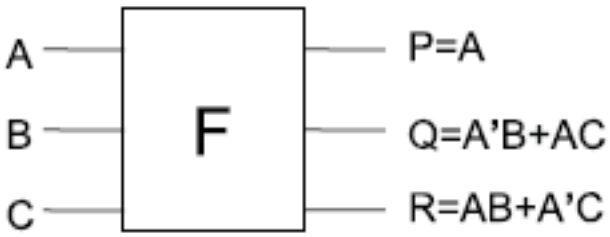

Figure 5: Fredkin Gate

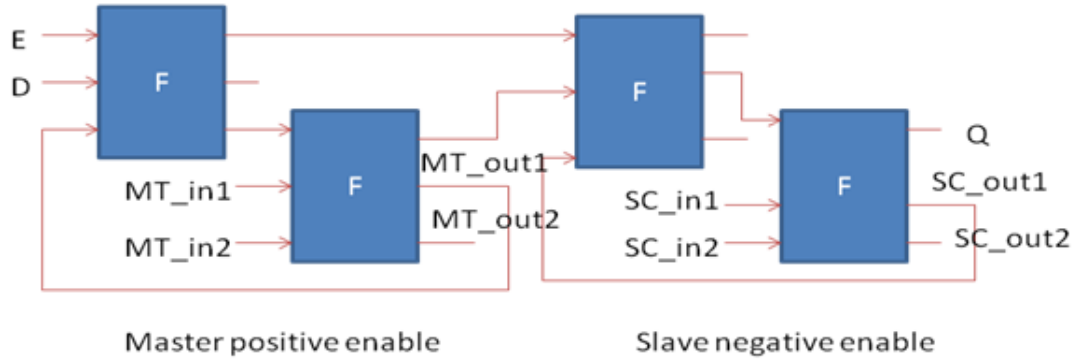

Figure 6: Master Slave Flip-flop Using Testable Reversible Logic Gates

The testable reversible D flip-flop [9] has four control signals ST_in1, ST_in2, MT_in1 and MT_in2. The MT_in1 and MT_in2 control the modes for the master latch while ST_in1 and ST_in2 control the modes for the slave latch module. In the normal mode when the design is working as a master-slave flip-flop the values of the controls signals will be MT_in1 = 0 and MT_in2 = 1 and ST_in1 = 0 and ST_in2 = 1. To check for any stuck-at-faults values for control signals can be other than these values.

IV. RESULTS

The proposed design has developed using Verilog HDL and simulated results have obtained from Model-sim. And the synthesis has done by XILINX ISE and implemented into SPARTAN 3E FPGA device and hardware results have been captured from CHIPSCOPE pro analyzer tool.

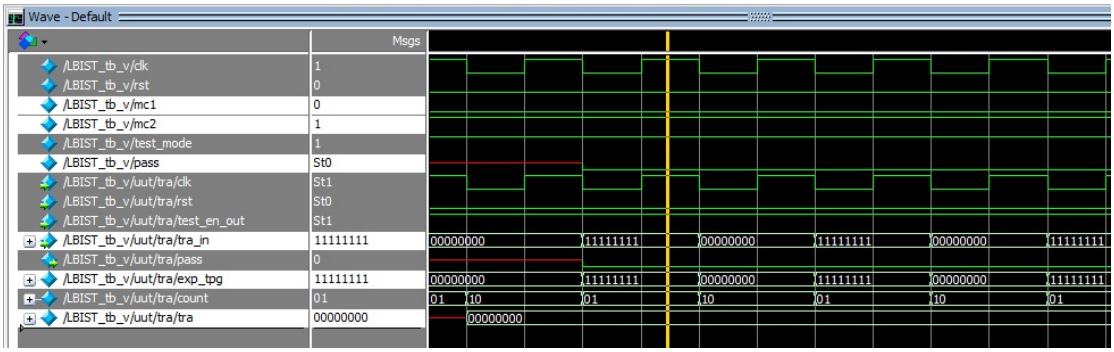

Figure 7: Simulation of LBIST using Conventional Flip-Flops

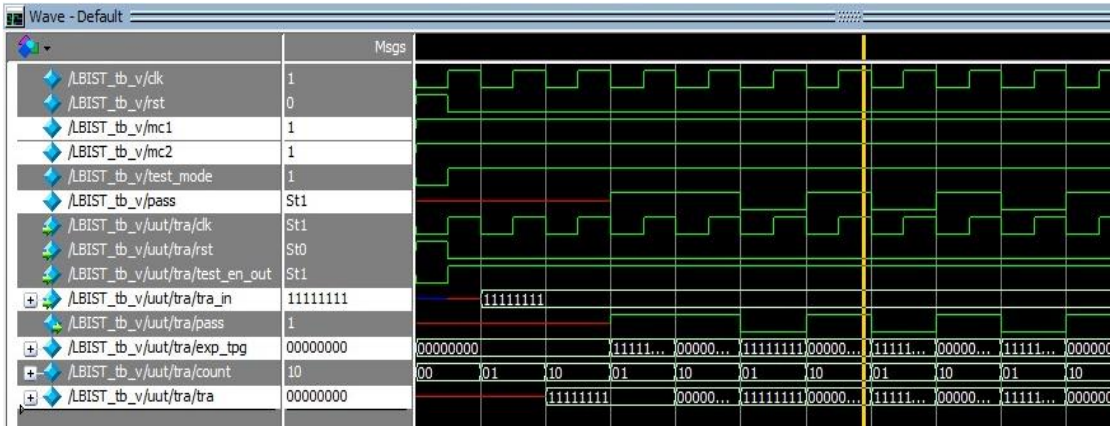

Figure 8: Simulation of LBIST Using Testable Reversible Logic Flip-Flops

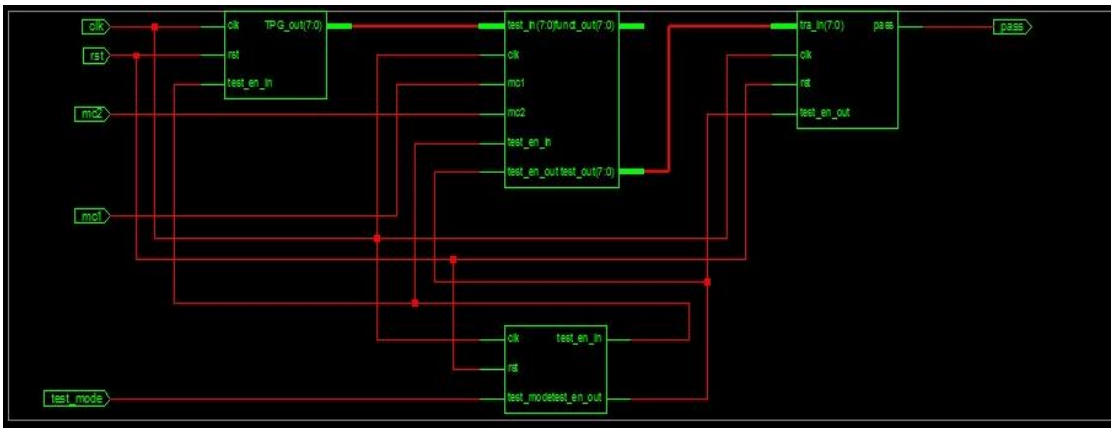

Figure 9: Schematic of LBIST obtained from XILINX XST Tool

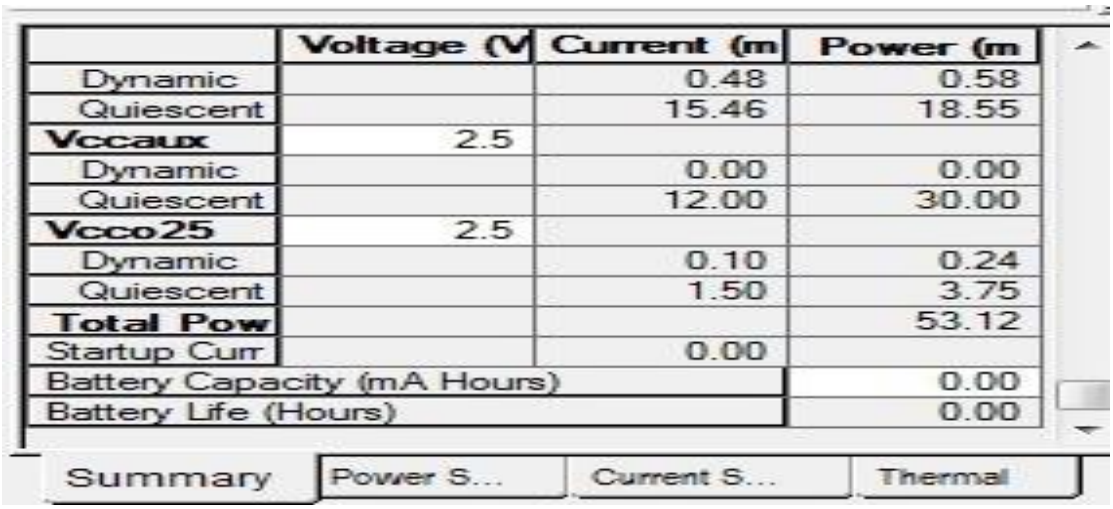

Figure 10: Power for Existing System

	Voltage (V)	Current (mA)	Power (mW)
Vccint	1.2		
Dynamic		0.22	0.26
Quiescent		15.46	18.55
Vccaux	2.5		
Dynamic		0.00	0.00
Quiescent		12.00	30.00
Vcco25	2.5		
Dynamic		0.09	0.24
Quiescent		1.50	3.75
Total Power			52.80
Startup Current (mA)		0.00	
Battery Capacity (mA Hours)			0.00
Battery Life (Hours)			0.00

Figure 11: Power for Proposed System

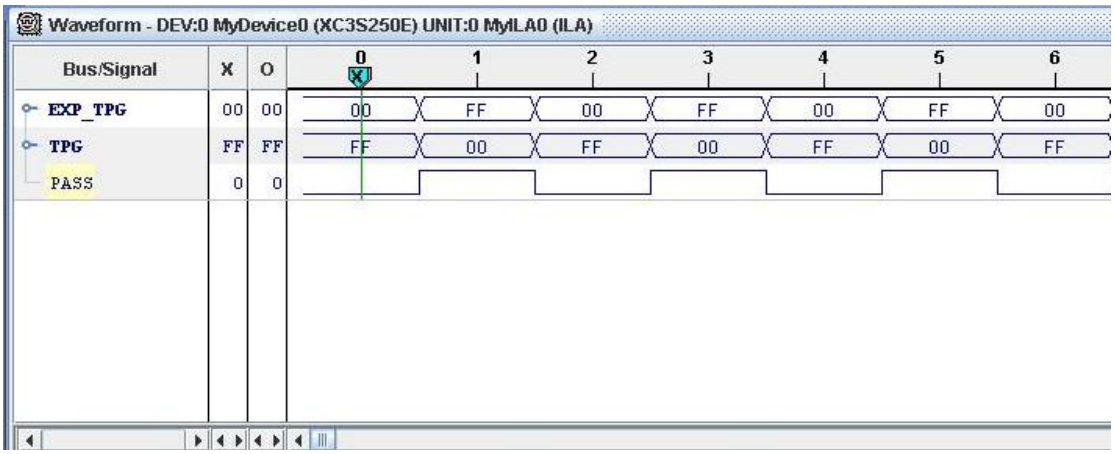

Figure 12: Chip Scope Result for Proposed System

Table 2: Power Report

Implementation Style	Total Power (in mW)
Conventional FF	53.12
Reversible Logic FF	52.70

CONCLUSION

The feedback shift register has designed using testable reversible sequential logic primitive D flip-flop which has the control signals to test. The testable reversible sequential logic primitive D flip-flop has designed using basic reversible logic gate named as FREDKIN gate. The efficient scrutiny equipment LBIST has designed to provide inputs for control signals and verify the functionality of FSR. The proposed design has developed using Verilog HDL and simulated results have obtained from

Model-sim. And the synthesis has been done by XILINX ISE. Hence, we have observed that the proposed design has required low power. The proposed design has implemented into SPARTAN 3E FPGA device and hardware results have captured from CHIPSCOPE pro Analyzer tool.

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