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FPGA Implementation of Variable Bit Rate 16 QAM Transceiver System

S. Dhanasekar[1], Dr. J. Ramesh[2]
[1] Part Time Research scholar, Department of ECE, PSG college of Technology, Coimbatore.
[2]Assistant Professor(SG), Department of ECE, PSG college of Technology, Coimbatore.
[1]Email: dhanasekar.sm@gmail.com [2]Email: jramesh60@yahoo.com

Abstract

FPGA chips are Field-upgradable, reliable in designing and implementation. The FPGA Technology has been playing a significant role in mobile communication. In this paper, a Variable Bit Rate 16 QAM Transmitter and Receiver has developed and implemented using FPGA. The Proposed architecture is transmitted over different input Bit patterns and modulated by variable clock frequencies. The implemented system is presently used in Digital terrestrial television using DVB-Digital Video Broadcasting and WIFI Networking Standards. Compared to the other Modulation Techniques, 16 QAM saves the Bandwidth with less Bit Error Rate. The 16 QAM Transceiver blocks consist of Source Encoding, Numerically Controlled Oscillator (NCO), Low pass filter, Gray coding and Signal Amplitude Detection. This Modulation scheme is coded using Verilog HDL and it is synthesized and simulated using Xilinx ISE and Modelsim tool. Xilinx Spartan3 xc3s200-5 PQ208 FPGA board will be used for testing and demonstration of the implemented system. The design spends about 85.8K gates and consumed Power is about 37mW with the operating frequency of 81.2MHz.

Keywords: QAM, OFDM, NCO, FPGA.

I. Introduction

Due to the tremendous development in modern communication technology, the requirement for authentic high date rate transmission is increased significantly, which accelerate much interest in modulation schemes. In each Modulation technique, the number of bits per symbol is changed.Quadrature Amplitude Modulation (QAM) is an efficient modulation scheme used widely to maximize the throughput and saving the Bandwidth. In this paper, a 16 QAM Transceiver system is employed for carrying

digital information over a Band-pass channels to save bandwidth. In 16 QAM modulation scheme, two sinusoidal carriers are precisely 90 degrees out of phase with each other are used to transmit data over the physical channel. The two sinusoidal carriers are orthogonal to each other because of the 90 degree phase shift can be can be modulated independently through the same frequency band and separated by demodulation at the receiver. It is a popular digital modulation technique in which both phase and amplitude are varied and it has basically developed to overcome constraints of complex AM and PM. In 16-QAM, a total of 16 possible states (symbols) and each symbol consist of four bits (i.e) two bits for I and two bits for Q components. As compared to other QAM, it can deliver less Bit Error Rate (BER), the low noise effect and it can carry more bits per second with minimal usage of Bandwidth.

Orthogonal frequency division multiplexing (OFDM) is able to achieve a highly efficient form of Multi-carrier Modulation which is widely used in Broadcasting, ADSL and Wireless Engineering. OFDM is the effective modulation technique that can provide large data rates depends on the requirement. The 16 QAM Modulation scheme is used in OFDM for Data Transmission. The WiFi radio signals enables higher data rates due to OFDM coding techniques. With WIFI, due to the OFDM coding technique we can save the bandwidth and enhance the data rate of the signal. In WiFi networking technology, radio signals are used for Data transmission. It is precisely alike to walkie-talkies, but the only difference is being on the strength of signals. A standard walkie-talkie can hold only confined data in the extend of 1000 bits per second and operate at 49MHz. In WiFi radios, the signal strength is more hence they can cover high data rate and it operates up to 5GHz frequency.

The FPGA Technology offers more flexible, reliable and accurate in simulating, testing, validating and implementing the designs. The 16 QAM Transceiver system is coded using Verilog HDL, simulated and synthesized using Modelsim and Xilinx tool and it is implemented using a Spartan3 FPGA Board. The paper is organized as follows. First, a brief review of 16 QAM Transceiver Design is described in Section II. The Results for 16 QAM Transceiver system are discussed in section III. Finally, concluding remarks are presented in section IV.

II.16 QAM Transceiver Design

The Digital Data Generator is provided with Variable data length and it will flow through serially as an input to QAM transmitter. The two carrier waves, Inphase (I) and Quadrature phase (Q) components can be represented as:

$$I(t) = a\cos 2\pi f_c t \qquad (1)$$

$$Q(t) = b\cos 2\pi f_c t \qquad (2)$$

Where I (t) and Q (t) are the modulating signals and f_c is the carrier frequency.

In 16 QAM Modulation technique, transmitted data are varied by both amplitude and phase of the carrier signal. Two carrier waves are used which are orthogonal to

each other. There are 16 possible states (symbols) and each symbol consist of four bits (i.e) two bits for I and two bits for Q components. The general form of a 16 QAM signal can be defined as:

$$TX(t) = \sqrt{\frac{2Emin}{Ts}}\, ai \cos 2\pi f_c t + \sqrt{\frac{2Emin}{Ts}}\, bi \cos 2\pi f_c t$$

$$0 \leq t \leq Ts;\ \ i = 1,2,3,4 \ldots \ldots 16 \qquad (3)$$

Where E_{min} is the energy of the signal with the lowest amplitude and a_i and b_i are a pair of independent integers chosen according to the location of the particular signal point. fc is the carrier frequency, Ts is the symbol period.

A. 16 QAM Transmitter Design

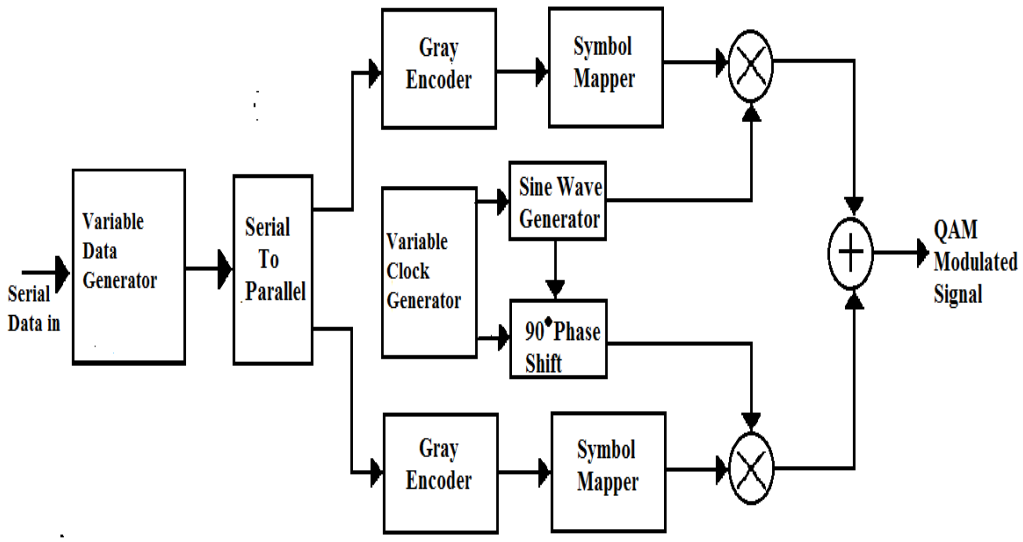

Fig. 1. QAM Transmitter Design

The Variable Pattern Generator or Data Generator is a basic requirement for digital circuit analysis. It is used in Digital Communication as a data source. The Digital Data Generator is provided with Variable data length (8,16,32 and 64 bits) will flow through serially as an input to QAM transmitter. The serial data is encoded by four bits and it is divided into two streams as Inphase (I) & Quadrature (Q). I values are called as odd sequence as it following odd values of the Data pattern. Q values can be called as even sequence as it follows even values of the Data pattern. The results from the Inphase (I) and Quadrature (Q) components are sent to Gray Encoder Block to minimize the Bit Error Rate (BER) for a given symbol error rate. Then the Inphase (I) and Quadrature (Q) components are multiplied with variable clock frequencies of sine and cosine carriers to get my Modulation and Q Modulation and it's got added to form QAM Signal.

B. Symbol Mapper For 16 QAM Transmitter Design

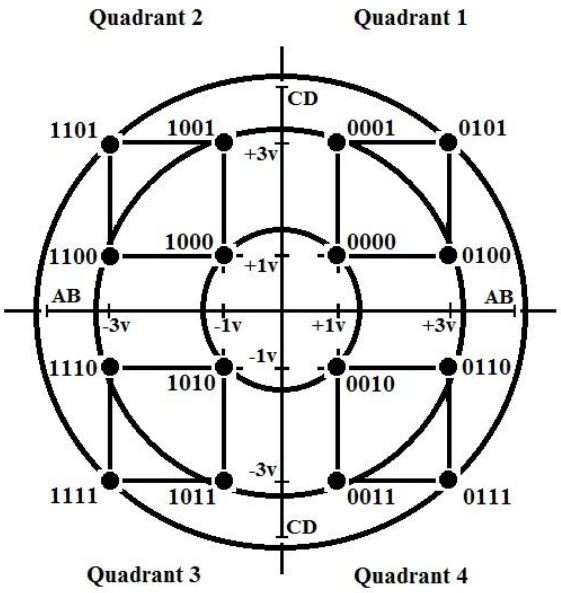

Fig. 2. Constellation diagram for 16- QAM

A Constellation Diagram is a plot of the symbols of the rectangular space. The 16 QAM Modulation Signal is the combination of I channel and Q channel. It has 16 symbols, each symbol consists of 4 bits (i.e. I – 2 bits and Q- 2 bits) is explained in the constellation Diagram Fig 2. The 16 QAM has 4 Amplitudes and 12 phases. The I and Q values can take four discrete values: ±3, ±1. In the 16-QAM, the number of amplitude shifts is lesser than the phase shifts. This is because the amplitude changes are susceptible to noise and require greater shift differences. The phase shifts used by QAM system are larger than the amplitude shifts.

C. 16 QAM Receiver Design:

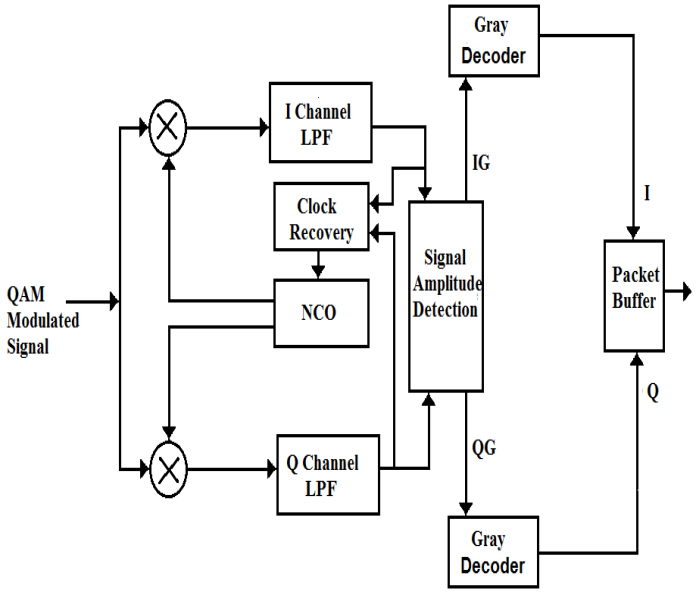

Fig. 3. QAM Receiver Design

The QAM Receiver (Demodulator) takes the modulated output from a transmitter signal as input and it is multiplied with NCO generated sine and cosine carriers to get I Demodulation and Q Demodulation Signals. The Results from the I Demodulator and Q Demodulator signals are sent to Low pass filter to attenuate the high frequencies and pass them into low frequency. When the data gets filtered in the Demodulator, it will flow through Signal Amplitude Detection to the group data range and obtain transmitted data. Hence, the results from the signal amplitude Detection have two bits of IG & QG send to Gray Decoder. The results from the Gray Decoder block consist of two bits of I & Q and it will flow through the Four bits Decoding, which is used to Decode I & Q Bits into serial data.

III. Results and Discussions

A. Variable Clock Generator

The Clock Generator works with Variable Step Frequencies (1.2KHz, 2.4KHz and 19.2KHz) can be controlled using DIP switches in FPGA.

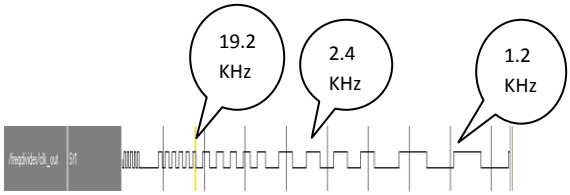

Fig. 4. Variable Clock Generator

B. Variable Pattern Generator

Data Generator is provided with Variable data length (8,16,32 and 64) Bit Pattern of different length can be selected using DIP switches in FPGA. The Simulation Results shown in Fig.5. is for 32 Bit Pattern.

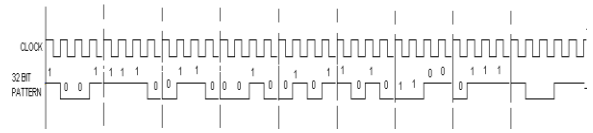

Fig. 5. 32-Bit length Data pattern

C. Serial To Parallel Converter and Gray Encoder

Four Bit Encoded data is similar to the data output from the data pattern generator and it is divided into two streams as Inphase (I) & Quadrature (Q). I stream is called as odd sequence as it following odd values of the Data pattern. Q stream can be called as even sequence as it following even values of the Data pattern. The frequency of the data after encoding will be $1/4^{th}$ of clock generator.

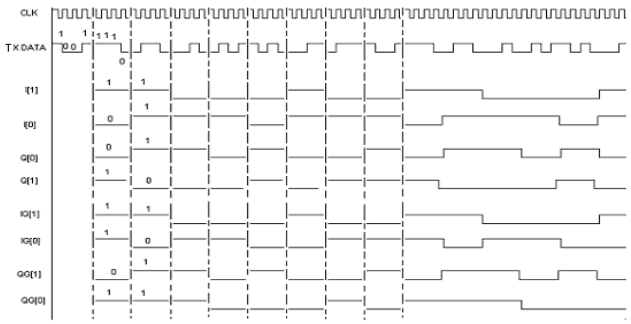

Fig. 6. Gray coded outputs for I & Q

D. I-Q Channel Symbol Mapper

In 16 QAM, $16= 2^4$, four bits per symbol can be sent. It consists of two bits of I component and two bits of Q component. The I Channel and Q Channel is used to modulate respectively by sine and cosine carrier signals.

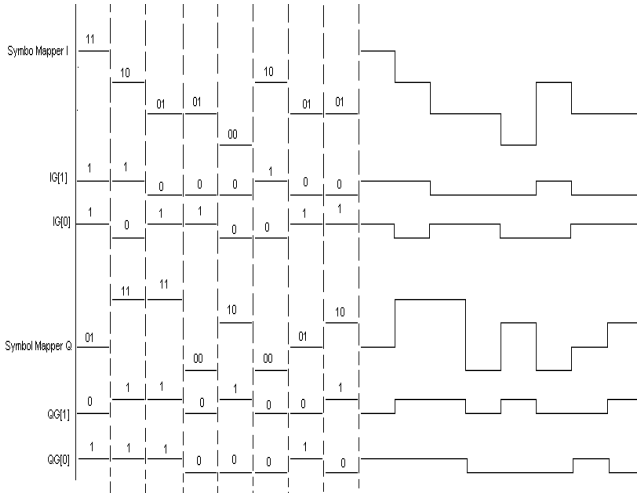

Fig. 7. Symbol Mapper outputs for I & Q Channel

E. Constellation Diagram for I-Q Channel

The X-axis projection for each symbol is the I Channel amplitude and Y-axis projection for each symbol is the Q Channel amplitude.

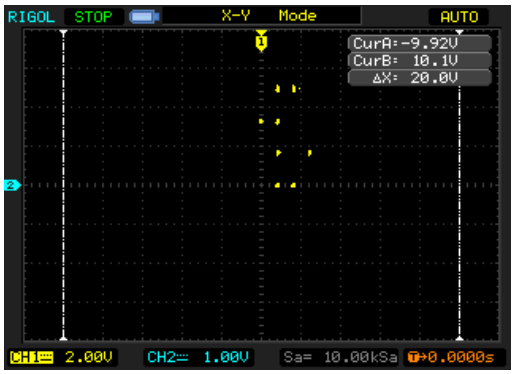

Fig. 8. Constellation Diagram for I-Q Channel

F. 16-QAM Modulation

The 16 QAM Modulation signal is the combination of I channel and Q channel. It has 16 symbols, each symbol consists of 4 bits (i.e. I - 2 bits and Q- 2 bits) is explained in the constellation diagram.

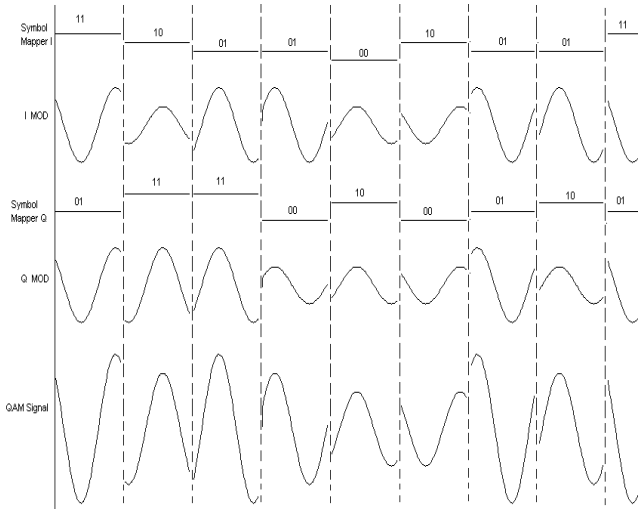

Fig. 9. 16-QAM Modulation Signal with Variable Data

G. 16-QAM Demodulator

The QAM Receiver (Demodulator) takes the modulated output from the transmitted signal as input and it is multiplied with NCO generated sine and cosine carriers to obtain I Demodulation and Q Demodulation Signals.

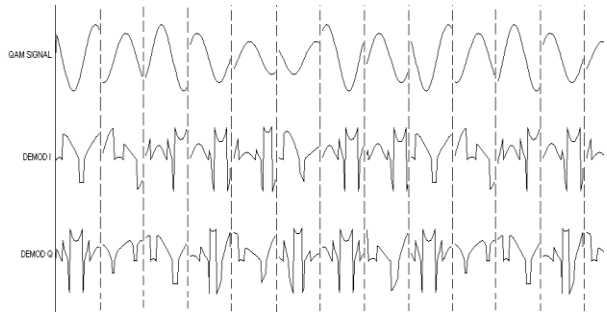

Fig. 10. Sine and Cosine Demodulator

H. Symbol Demapper and signal Amplitude Detection

The Results from the I Demodulator and Q Demodulator signals are sent to Low pass filter to attenuate the high frequencies and pass them into low frequency. By means of Low pass filter,we can reduce the Noise and Intersymbol Interference (ISI) in the received data.

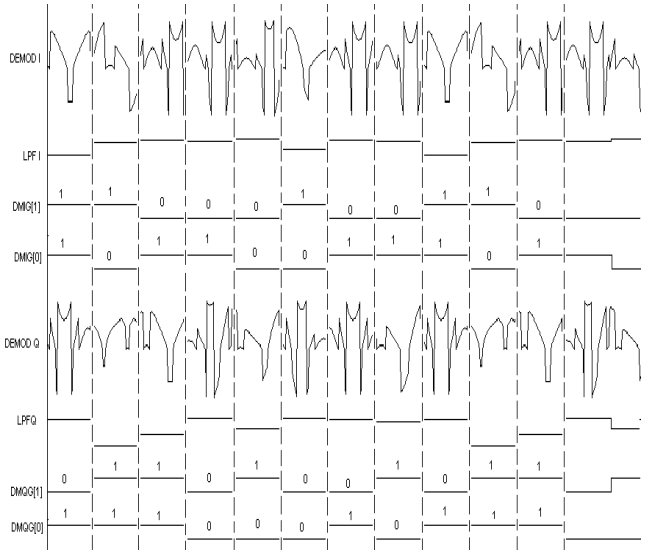

Fig. 11. Demodulated Outputs I Channel and Q Channel for Low Pass Filter and Signal Amplitude Detection

I. Gray Decoding

The results from the signal amplitude Detection have two bits of IG & QG are sent to Gray Decoder. The Gray Decoder is used to decode the Gray data into Binary data to obtain transmitted data in the receiver. Four Bit Decoded data is similar to the encoded process in the transmitter.

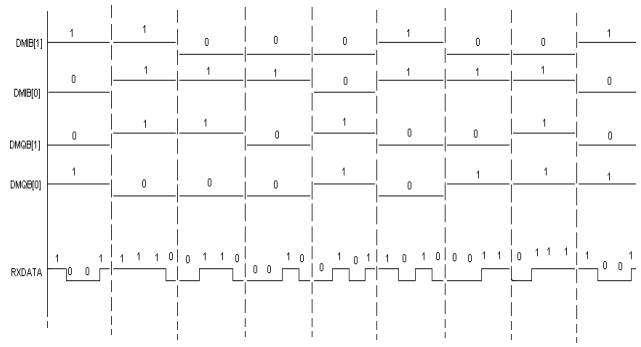

Fig. 12. 4 Bit Decoding output

J. 16-QAM Transmitter and Receiver system

The serial bit data given to the 16-QAM Transmitter and Packet Buffer are obtained in receiver are compared.

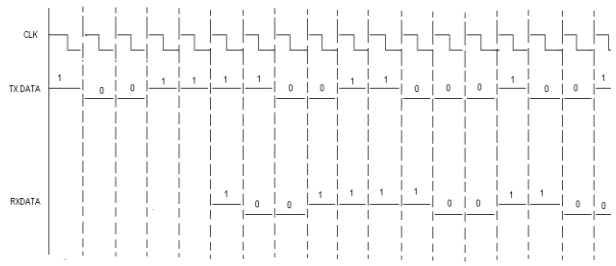

Fig. 13. Output of Transmitter and Receiver Data

The Functional simulation of the proposed architecture has been justified by using Verilog HDL. The various parameters obtained from 16 QAM Transceiver system are listed in Table 1.

Table 1. 16 QAM Transceiver Output

Gate count for design	Estimated Power Consumption	Minimum period	Maximum combinational path delay
85,875	37mW	12.3ns	6.36ns

The Proposed Architecture are synthesized and simulated using Xilinx ISE, Modelsim tool and Spartan3 xc3s200-5pq208 FPGA device chip. The Device utilization summary is listed in Table 2.

Table 2. Device Utilization summary - Spartan3 FPGA Board

Logic utilization	Used	Available	Utilization
Number of Slices	686	1920	35 %
Number of 4 input LUTs	1276	3840	33%
Number of bonded IOBs	115	141	81%

IV. Conclusion

This paper describes the step by step journey of the signals from source to destination of the 16 QAM Transceiver system. It is a popular digital modulation technique in which both phase and amplitude are varied and it used for OFDM applications. This type of Modulation is used to obtain high data with low noise effect and less Bit Error rate compared to other QAM. The Proposed architecture is transmitted by giving different input Bit patterns and modulated by means of various clock frequencies. The 16 QAM Transceiver system is coded using Verilog HDL, simulated and synthesized using Modelsim and Xilinx tool and implemented using Spartan3 FPGA Board. Our design consumed the power is about 37mW with the operating frequency of 81.2 MHz.

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