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# Design of An Optimized Fir Filter For Signal Processing Applications

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## Abstract

Signal processing applications have become very popular due to the use of digital filters. Among digital filters FIR filters are opted due to its stability and response which is finite. In this paper a low power and high speed FIR filter is designed. The filter is pipelined which will reduce the critical path. So high speed is achieved and consumption of power is reduced. Then parallel processing of the filter is done which duplicates the hardware. Hence many outputs can be calculated in parallel which will increase the speed of the filter. Canonical signed digit (CSD) representation is used in which the numbers of non-zero coefficients are reduced. This will decrease the transitions hence power consumption is less. The designed filter is simulated in Modelsim-altera 10.1d and synthesized in Xilinx ISE 13.2.

**Keywords:** FIR, pipelining, parallel processing, CSD

## Introduction

A digital filter plays a substantial role in digital signal Processing (DSP) applications [3].The use of digital technology is rising dramatically and many audio, video and cellular industries depend in digital technology. Hence digital filters are important in digital applications [6]. The unwanted frequency components from the signals are removed using digital filters and the wanted signals can be enhanced. Digital signal processing applications have become popular due to the use of digital filters.

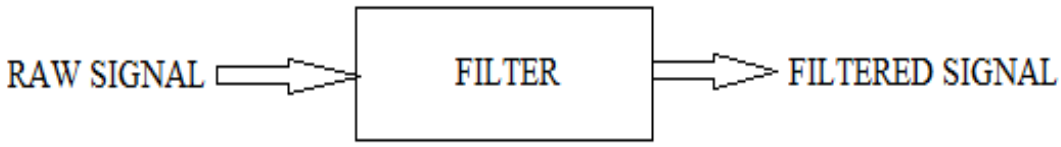



**Figure 1:** Basic filter block

The digital filters are advantageous because they are easily programmable and can be designed and implemented easily. Since it is programmable it does not affect the hardware circuitry so redesigning of the circuit is not required. Digital filters are more accurate compared to analog filters and have high tolerance to component variations.

Signal separation and restoration is the two uses of digital filters [4]. When a signal has been corrupted with noise or other signals signal separation is needed. The retrieval of signals when it gets distorted is done using signal restoration.

## FIR Filters

The digital filters have 2 types: Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) filters [3]. The first type i.e. IIR are recursive filters. Their output depends on the previous output values in addition to the input values. IIR filters can be used only when the system has infinite response. So it requires more processing time. It has no phase and the delay adjustment makes it unstable [6]. It also requires large number of multiplication operations and addition operations compared to FIR filter [3].

The FIR filters are non-recursive filters. Their output can be determined from the present and past input values. It can be used for higher order tapping. It has finite response and requires less number of additions and multiplications. It is stable and has a linear phase. Hence FIR filters are preferred over IIR filter because it is more stable and has no feedback.

The general FIR filter equation is,

$$y(n) = b(0)x(n) + b(1)x(n-1) + \ldots + b(n)x(n-N) \quad (1)$$

$$= \sum_{i=0}^{N} b(i)x(n-i)$$

where output of filter at discrete time instance n is y(n), the input of the filter is x(n), coefficient of the filter is b(i) and order of filter is N.

The FIR filters are simplest filter since it can be designed easily. After a finite time the output of the FIR filter becomes zero if a single impulse is present at the input and all other successive inputs are zero. The filter coefficients number is the time needed for the filter output to become zero.

The general structure of an FIR filters is,

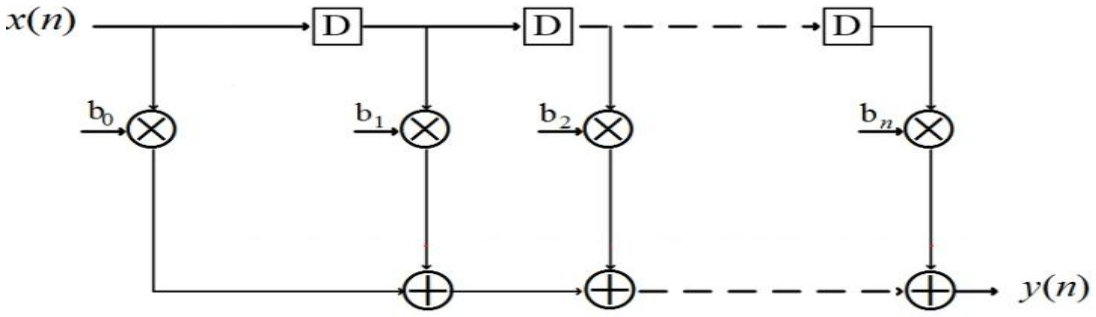



**Figure 2:** Basic FIR filter

## Existing System

**Direct Form (DF) Fir Filter:**
Structures in which the multiplier coefficients are the coefficients of the transfer function are called direct form structures [4].

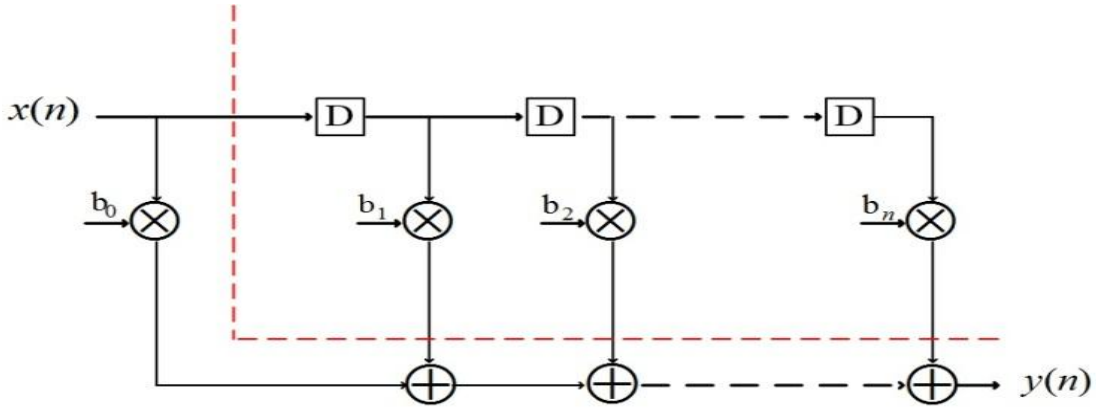



**Figure 3:** DF FIR filter block diagram

**Direct Form Fir Filter Using Pipelining:**
The latches are inserted down the data path in pipelining. The advantages of pipelining are [5]:

- Critical path gets reduced.
- Clock speed or sample speed gets raised.
- Power consumption is less.

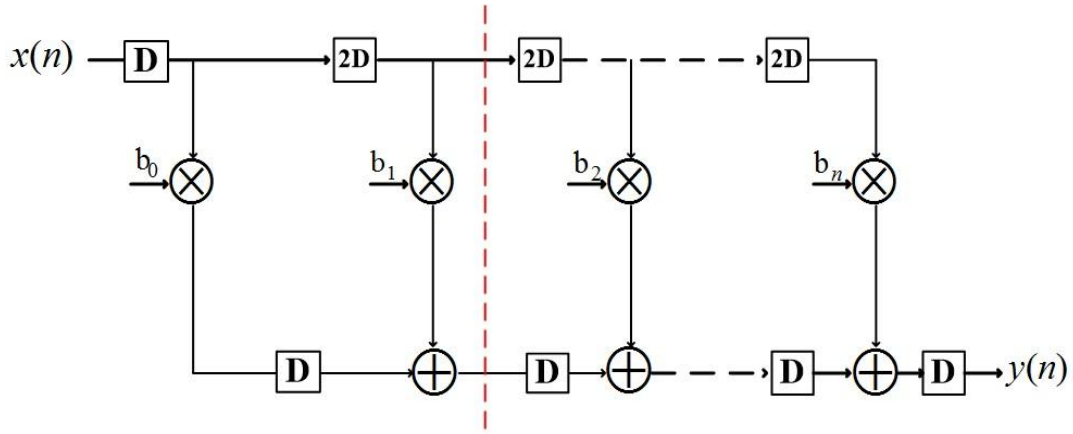



**Figure 4:** DF block using pipelining

In pipelining many functional units can be run simultaneously. So the throughput of the system will be enhanced while processing the functional units.

The propagation delay of the sequential filter is given by,

$$T_{pip} = \frac{\frac{c_{charge}}{M}\beta v_o}{k(v_o - v_t)^2} \tag{2}$$

The pipelined filter has propagation delay of,

$$T_{pip} = \frac{\frac{c_{charge}}{M}\beta v_o}{k(v_o - v_t)^2} \tag{3}$$

where the critical path decreases to 1/M of the actual length [5] .

The power consumption of the sequential filter is,

$$p_{seq} = c_{total} v_o^2 f \tag{4}$$

The power consumption of filter that is pipelined is,

$$p_{pip} = c_{total} \beta^2 v_o^2 f \tag{5}$$

$$p_{pip} = \beta^2 T_{seq} \tag{6}$$

## Proposed System

### Transposed Direct Form (TDF)

The TDF of a FIR filter can be obtained by variations in the DF filter. The TDF can be created from the DF by the consequent steps:

- The input signal and output signal are interchanged.
- Signal flow direction is reversed.
- The summing node becomes branching node and vice versa.

After this, the input signal will be present on the right side of the graph. To make it standardized again the whole graph is left-right swapped. The functionality of the system does not get changed by transposing the filter.

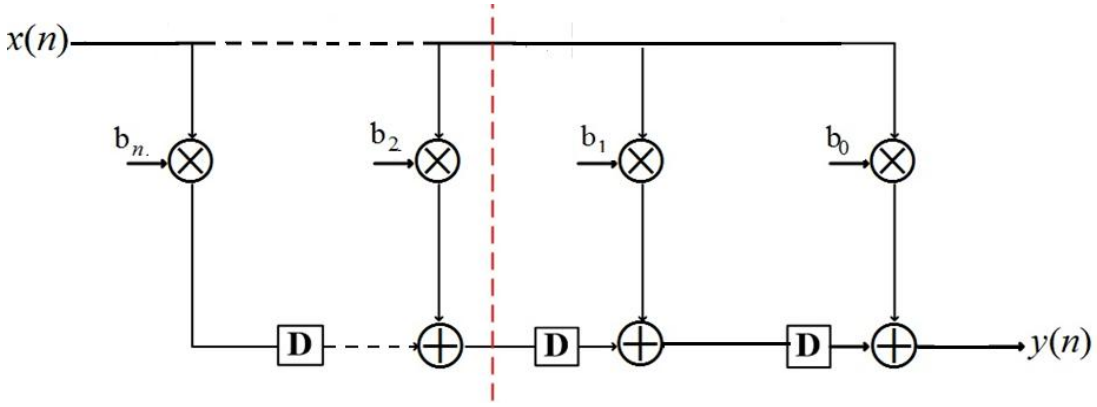



**Figure 5:** TDF block diagram

**Transposed Direct Form Fir Filter Using Pipelining:**

The latches are inserted down the data path in pipelining. The advantages of pipelining are [5]:

- Critical path gets reduced.
- Clock speed or sample speed gets raised.
- Power consumption is less.

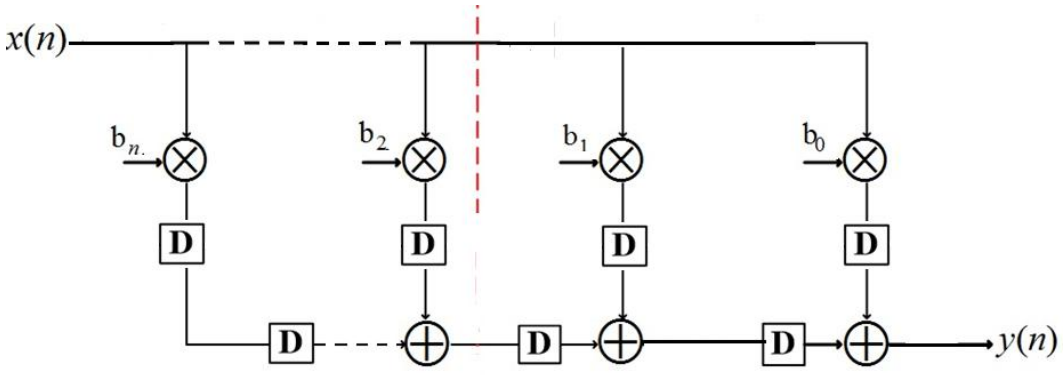



**Figure 6:** TDF pipelined block

**Transposed Direct Form Using Parallel Processing**

Pipelining and parallel processing are pairs of each other. If a system can be pipelined then parallel processing can also be done to it. The hardware is duplicated in parallel processing. The advantages of parallel processing are:

- The sample speed is increased.
- Power consumption is reduced.

A single-input single-output (SISO) system is converted to a multi-input multi-output (MIMO) system. In a clock period many outputs can be calculated in parallel [5].

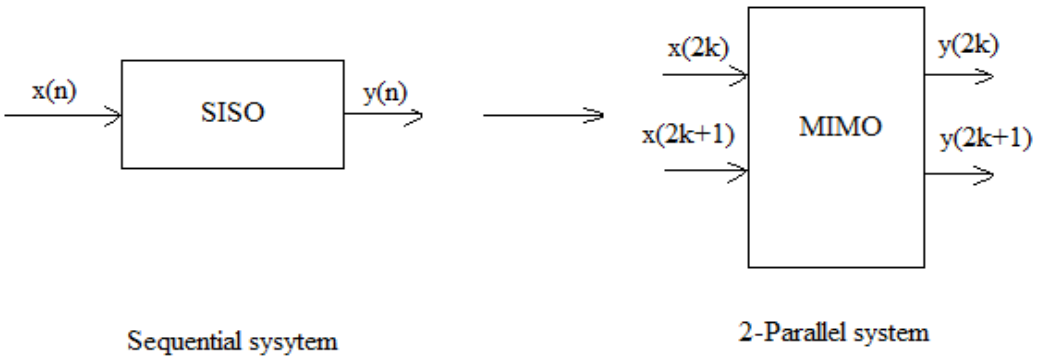



**Figure 7:** Parallel Processing Block

A SISO FIR filter is given as,

$$s(n) = px(n) + qx(n-1) + rx(n-2) \tag{7}$$

Converting it into a parallel processed MIMO design with level 2,

$$s(2l) = px(2l) + qx(2l-1) + rx(2l-2) \tag{8}$$

$$s(2l+1) = px(2l+1) + qx(2l) + rx(2l-1) \tag{9}$$

The propagation delay of a parallel processed system is,

$$LT_{seq} = \frac{c_{charge}\beta v_o}{k(\beta v_o - v_t)^2} \tag{10}$$

The power consumption is given by,

$$p_{par} = (LC_{charge})(\beta v_o)^2 \frac{f}{L} \tag{11}$$

$$= \beta^2 p_{seq}$$

**Fir Filter Using CSD**

The Canonical Signed Digit (CSD) is a unique representation based on ternary number system [2]. The numbers of non-zero coefficients are reduced by encoding the binary number. Since the representation has minimum non-zero bits it is called canonical. The numbers of partial products are thus reduced when the number is multiplied with the coefficients [1]. The digit can be a +1, 0 or -1 in CSD representation. The string property is utilized in representing a number in CSD form. It identifies strings of 1s as it moves from least significant bit (LSB) to most

significant bit (MSB) and substitutes the strings with its equivalent value of +1, 0 or -1.

The CSD representation is an important method of radix-2 signed digit representation. It has properties which are mentioned below [1]:

1. Two successive bits in the number should not be non-zero.
2. The CSD is a unique representation.
3. The non-zero digits that are present are minimum.

In multiplication the shift and add algorithm is used while in CSD representation it is changed into shift and add/subtract algorithm. First the strings of 1s are identified. The LSB of the string is changed to $\bar{1}$ and all other numbers are converted into zeroes. The MSB of the number is changed to 1. The number is studied for other strings of 1s. If it is present then the process is repeated again until no strings are identified.

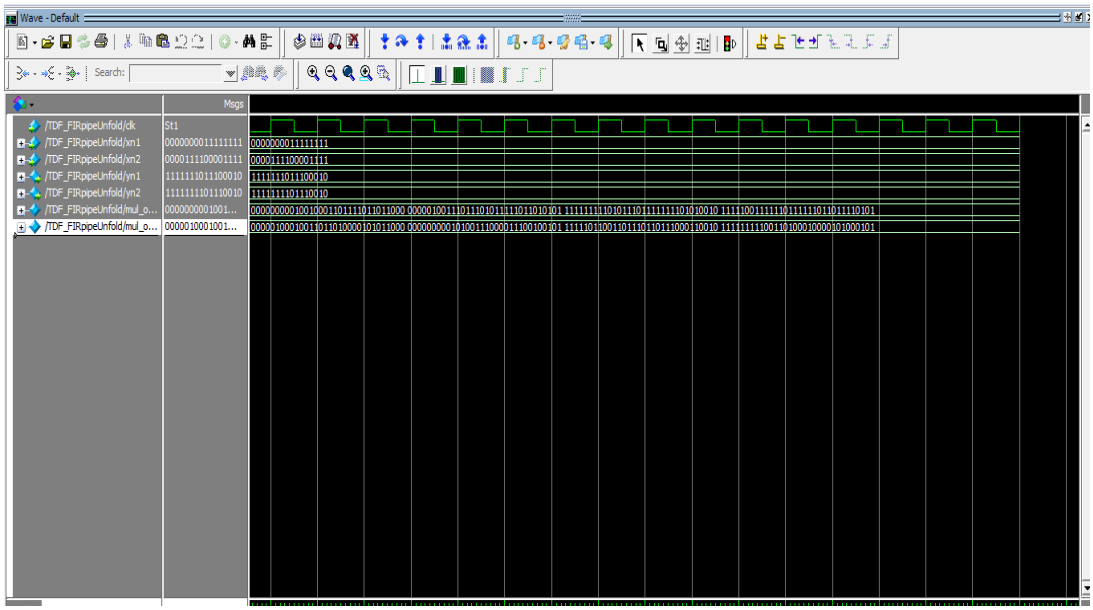
A number X with length N has the value as [7],

$$x = \sum_{i=0}^{N-1} x_i 2^i \tag{12}$$

where $xi \in \{-1,0,+1\}$.

The use of Canonical Signed Digit (CSD) representation makes the multiplication process faster since the numbers of partial products are reduced. Due to the reduction in the partial products the number of adders that are needed to be used is also decreased which reduces the area needed.

## Simulation Result



**Synthesis Report:**

No of slices: 160
No of slice flip flops: 272
No of 4 input LUTs: 192
No of bonded IOBs: 65
No of MULT 18X18SIOs: 8
No of GCLKs: 1

**Timing Details:**

Speed Grade: -5
Minimum period: 4.932ns
Maximum frequency: 202.757MHz
Minimum input arrival time before clock: 1.976ns
Minimum output required time after clock: 4.040ns

## Conclusion

A low power and high speed FIR filter is designed. The filter is pipelined to reduce the critical path and parallel processed to save time. The CSD method is used to decrease the power consumption of the filter. The design is simulated in Modelsim-Altera 10.1d and synthesized using Xilinx ISE 13.2 and the results are compared.

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