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Hardware Implementation of All Digital Phase Locked Loop For Communication Applications

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Abstract

This paper proposes a novel design of All Digital FM receiver using All Digital Phase Locked Loop (ADPLL). Phase Locked Loop (PLL) is used to track the two signals. ADPLL has full of digital components. ADPLL is very important application in digital signal processing. It contains Numerically controlled Oscillator (NCO), Phase detector (PD), Loop filter. PD used as Booth encode Wallace tree so that speed is high and power consumption is low. MUX based NCO is used to reduce the area. By combining all block to construct the optimized All Digital Phase locked Loop (ADPLL). Transposed based pipelining and parallel processing FIR filter is used to increase the speed.

Key words: ADPLL, Phase Detector, NCO, FIR Filters.

Introduction

Phase locked loop (PLL) are feedback structure as long as initiate signals that are phase locked with external input signals. Phase locked loop operate as an oscillator to lock input signals in both phase and frequency. Both signals are synchronized in locked condition. Phase locked loop are widely occupied in radio, telecommunication and other electronic communications. It utilizes to demodulate the signal and retrieval from a noisy communication channel. Phase noise limits the wireless transceiver performance and the problem for digital processor is jitter[3]. The analog PLL implementation has many problematic applications and the cost of implementation is too high.

All digital phase locked loop [ADPLL] consist only of digital components. All digital PLL was first reported by Drogni [1967].All digital phase locked loop is extreme boon to communication system. ADPLL has upgrade portability, focused on system on chip applications and free from process deviation. The cost and time for this design also reduced. ADPLL enhance the testability, speed, reliability, performance and programmability of the circuits [1].

Description

This paper uses PLL is the main component for FM receiver in ADPLL. ADPLL has PD, loop filter and numerically controlled oscillator (NCO). PD determines the phase error between the input signals and output from NCO. A digital cosine waveforms are generated from the numerically controlled oscillator (NCO) for which frequency is determined by the input value. NCOs are used in many communication application includes radar system, digital PLLs, 3G wireless and software radio system. The input Frequency modulated signal comes from an 8 bit ADC (analog to digital) as a series of numerical values [2]. All Digital FM receiver circuit consists of Digital PLL and low pass filter and the block diagram shows in Fig1.

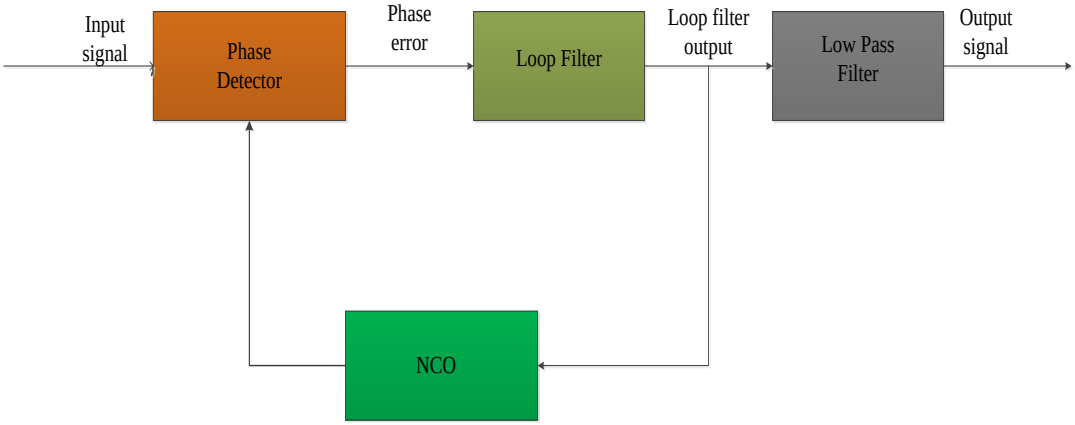

Figure 1: Block Diagram of ADPLL

Phase Detector (PD)

Existing Method

Phase error observed between two signals. Phase detector operates as a mixer [7]. Modified booth multiplier algorithm is used in phase detector.

Modified Booth Multiplier:

The Modified Booth multiplier (MBM) was proposed by O. L. Macsroley in 1961. In MBM there will be a reduction in partial products by half. Here only the second column is taken ±1, ±2 or 0 unlike in the other booth's multiplier, where every

column multiplier term was multiplied by 1 or 0. Groupings are performed and starts from LSB. The first pair use only two bits and assume zero for third bit. The greater number of bits can be examined and eliminated in which the product gets reduced [4].

Table 1: Modified Booth Multiplier

Q_{2i+1}	Q_{2i}	Q_{2i-1}	Recoded Digit
0	0	0	0
0	0	1	+1
0	1	0	+1
0	1	1	+2
1	0	0	-2
1	0	1	-1
1	1	0	-1
1	1	1	0

This table[1] shows the eight different states and these states get an outcomes of modified booth multiplier.Two bit numbers to be multiplied as P and Q, where Q is expressed as

(1) $Q = -Q_{m-1}2^{m-1} + Q_{m-2}2^{m-2} + \ldots + Q_0 2^0$

(2) $Q = (-2Q_{m-1} + Q_{m-2} + Q_{m-3})2^{m-2} + (-2Q_{i-3} + Q_{i-4} + Q_{i-5})2^{i-4} + \ldots + (-2Q_1 + Q_0 + Q_{-1})2^0$

Where $Q_{-1} = 0$, $Q_{i-3}2^{i-2} - Q_{i-2}2^{i-4} = Q_{i-3}$ used in above expression, eqn(2) can be represented in

$$Q = \sum_{i=0}^{i=m/2-1} (-2Q_{2i+1} + Q_{2i} + Q_{2i-1})2^{2i}$$

(3) $$Q = \sum_{m=0}^{i=m/2-1} Q_i - 2^i$$

(4) $$P.Q = -P_{m-1}2^{m-1} + \sum_{i=0}^{m-2} P_i 2^i \left(\sum_{j=0}^{m/2-1} Q_i 2^j \right)$$

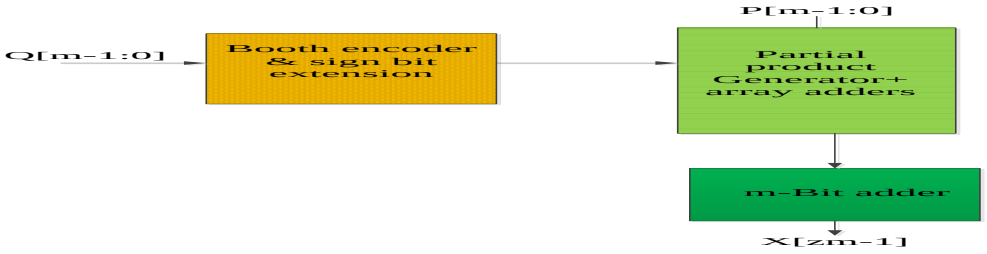

Figure 2: Modified Booth Multiplier Architecture

Proposed Method

Booth Encoded Wallace Tree Multiplier:
Booth encoded Wallace multiplier is the combination of both booth and Wallace tree multiplier (WTM). In WTM partial products are reduced and added into last two intermediate results. Adding these results by using carry look ahead adder to generate final output. Booth multiplier is an effective method to multiply signed binary numbers [8].

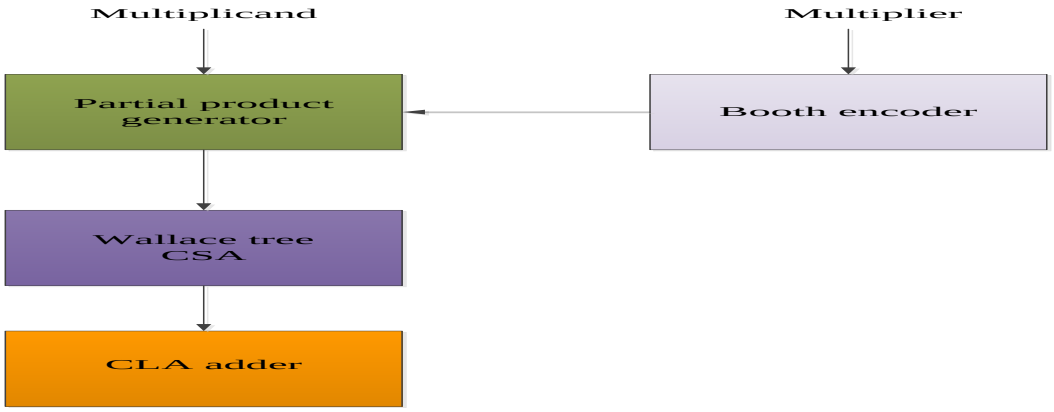

Figure 3: Booth encode Wallace tree Multiplier

Booth encodes Wallace tree multiplier is used in PD in which speed is high and power consumption is reduced. This effective multiplier is used in ADPLL to design a all digital FM receiver.

Numerically Controlled Oscillator (NCO):
An NCO generates a synchronous, discrete time and valued waveform like sinusoid, thus is basically digital signal generator. NCO has following blocks

- Phase Accumulator
- Phase to Amplitude converter

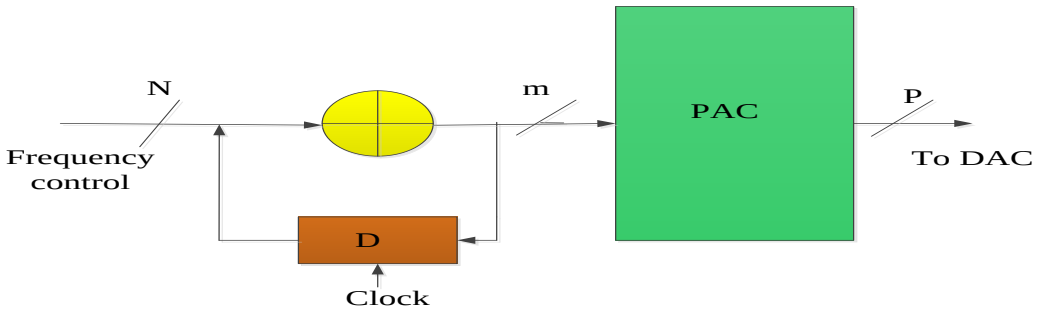

Figure 4: General block diagram of NCO

Consider two forms of NCO,

- Lookup table(LUT) based NCO
- Multiplexer (MUX) based NCO

Lookup Table Based NCO:

Figure 5: Block Diagram of Lookup Table based NCO

At every clock cycle, phase accumulator sum a phase _inc values are quantized before given to the LUT. Phase accumulator estimate angle value that is used to label the LUT for output waveform [9]

$$\theta_i = \theta_{i-1} + \Delta\theta$$

θ_i -- Phase angle at any cycle.

θ_{i-1} -- Last clock cycle.

Phase increment values are calculated by using,

(5) $\varphi_{inc} = (F_{out} . 2^{32}) / F_S + 0.5$

F_{out} -- Output frequency and F_S -- sampling frequency.

NCO generates maximum and minimum frequencies by using formulas,

$F_{max} = F_S / 2$ and $F_{min} = F_S / 2^{32}$

Multiplexer (MUX) Based NCO:

NCO output with a particular phase and frequency. LUT is used to store the first quadrant and the remaining bits(MSB) are used to shift the value or invert the value.

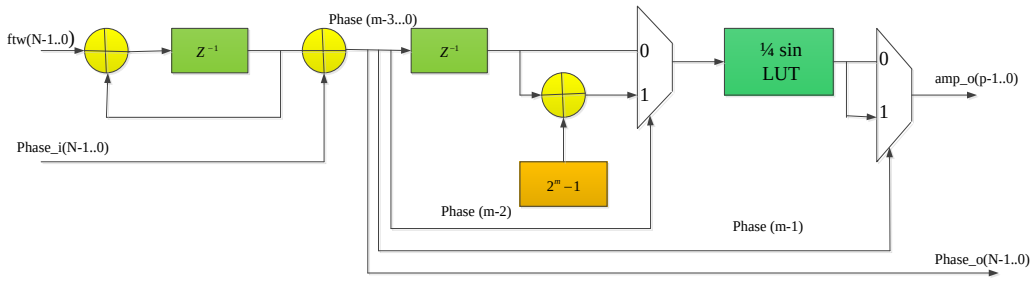

Figure 6: MUX based NCO

MUX based NCO is used in ADPLL for increasing speed and time reducing one because only the first quadrant values are calculated.

Fir Filters:

Finite impulse response is a nonrecursive filter with constant cofficient used in low pass filter[6]. The output for this filter of length L , y[n] is

(6) $y[n] = w[n] * x[n]$

$= \sum_{m=0}^{L-1} w[m]x[n-m]$ where $w[0] \neq 0$ and $w[L-1] \neq 0$ arefilter's coffiencients.

The transfer function of FIR filter is,

(7) $F[z] = \sum_{m=0}^{L-1} w[m]Z^{-m}$

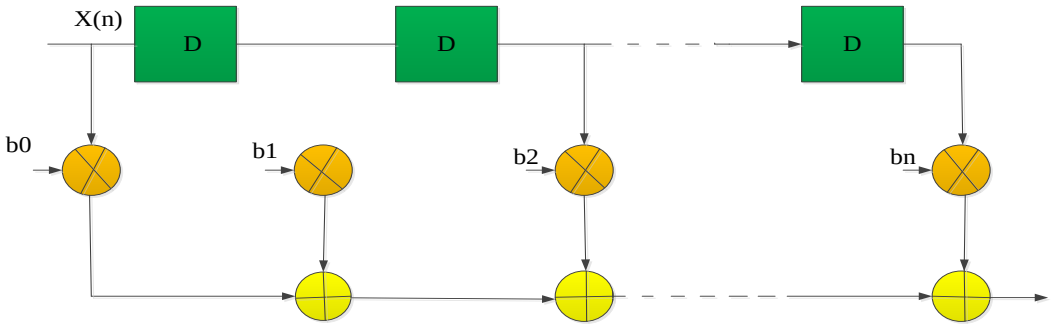

Figure 7: FIR Filter

Direct Form With Transposed Structure:

Transposed FIR filter is the variation of direct form model. It construct from direct form by

- Exchanging the input and output.
- Inverting the direction of signal flow.

Pipelining Fir Filter:

Pipelining FIR filter introduce latches along the datapath. clock speed is high and reduce the critical path. Power consumption also reduced.

Power consumption,

(8) $P_{pipe} = C_{total}\beta^2 v_0^2 f$

Propogation delay for this filter is,

(9) $T_{seq} = T_{pipe}$

After reducing the above eqn to get

(10) $M(\beta v_o - v_t)^2 = \beta(v_0 - v_t)^2$.

Parallel Processing

In Parallel processing FIR filter replicate the hardware in which sample speed is increased and also reduce the powe consumption.

Power consumption for parallel processing is,

$$P_{par} = (LC_{total})(\beta v_0)^2 f / 2 \quad (11)$$

Propogation delay,

$$LT_{seq} = T_{par} \quad (12)$$

Transposed Pipelining And Parallel Processing:

This method used in low pass filter to increases the speed of operation and reduces the power consumption, there is no need of increasing the sampling speed.

By combining the pipline and parallel processing to get,

$$LM.(\beta v_0 - v_t)^2 = \beta \quad (13)$$

Synthesis Report:

Area:

No of slice registers : 368
No of slice LUTs : 570
No of slice FF : 165
No of bounded IOBs : 22
No of BUFG/BUFRCTRLS : 1

Timing Details:

Speed Grade : -3
Minimum period : 6.002ns
Operating frequency : 166.600MHZ
Minimum input arrival time : 0.788ns

Conclusion

An ADPLL is designed using PD and NCO. It reduces area and has minimum hardware utilization. An all digital FM 1receiver which has low power and high speed designed using ADPLL. The circuit is simulated in Modelsim 10.1d and synthesized in Xilinx ISE 13.2.

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