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Performance Enhancement of MOS Transistor using Ge-Nano-wire Hetero junction Interband Tunnel Diode

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Abstract
In this paper, the high peak to valley ratio tunnel diode is embedded in the source region of partially depleted PD SOI n-MOSFET. An intrinsic germanium is introduced at different nano length in the source region of MOSFET. The result obtained is compared with different peak to valley ratios of embedded tunnel diode to obtain the constant saturated drain current for better output voltage swing. The other phenomenon's that originate from this device, such as low output resistance, capacitance, high voltage gain and distortion of output signal, were suppressed significantly. In addition, the proposed device Ge nanowire HTD PD SOI n-MOSFET is fully laid out and compatible with CMOS for high SNM. Proposed device can be considered as one of the promising candidate for low power digital and analog circuits. This structure is designed using COGENDA device Simulator and its performance is analyzed by I-V characteristics for different tunnel diode peak to valley ratio.

Keywords: HTD, Ge nanowire, HfO_2, Gain, Voltage Swing and Cut-off frequency.

I. INTRODUCTION

A tunnelling field effect transistor (TFET) is proposed as a promising candidate to extending metal–oxide–semiconductor FET (MOSFET). Earlier TFETs were gatecontrolled p–i–n diode where tunneling occurs along the gate-semiconductor interface. When this TFET is ON, tunneling occurs at the corner of the p+ source adjacent to the inversion channel, suffers from the area penalty. This device can also known as lateral TFET (LTTET) [8]. • Recently Seabaugh *et al*. proposed a vertical TFET (VTFET), where the tunnelling is perpendicular to the gate interface to increase the tunneling area. When the device is ON, electrons tunnel from the *p*+ source and is extracted to the drain through the n+ pocket underneath the gate [8]. S. sudirgo *et al*. proposed Resonant Interband Tunnel Diode (RTD) structure based CMOS structure where two tunnel diodes are connected in series with drain region of MOSFET to obtainhigh speed operation, large negative differential region (NDR) and 80% of voltage swing [10]. Sung–Yong Chung *et al*. discussed the voltage swing in SiGe resonant interband tunnel diode in which the impact of PVCR are shown respect to the voltage swing Since last two decade, partially depleted SOI (PD-SOI) has been proposed by several researchers for high-performance digital applications. Although PD-SOI MOSFET structure has been used successfully for a long time, it has certain disadvantages associated, like kink and hysteresis effect. Hence, the Jiex and Luo proposed the structure TDBC N-MOSFET for suppress the kink effect in which *p*+ is implanted in the *n*+ source region with equal distance. When the device is ON, electron tunnels through *p*+ source to the *n*-drain region, but in this approach there is a limitation of high doping in the *n*+ and *p*+ structure and not clearly visible in the tunnelling band structure of Tunnel diode. As the decreased channel length device does not work properly, this device is not suitable for nano meter regime [13]. Moreover, SOI MOSFET exhibits numerous advantages like, improvement in frequency performance due to the reduction in capacitance, high transconductance value, and reduction in interconnect length [9]. However, kink effect is the major concern in partially depleted SOI MOSFET, as a result better voltage swing is not able to obtain. For better voltage swing a new structure has been proposed that is Ge nanowire heterojunction tunnel diode (HTD) based PD SOI n-MOSFET in which Ge nanowire are embedded in source of MOSFET.

This paper proposes a possible solution that can suppress the kink effect of conventional MOSFET by means of a new type of device, which is referred as the Ge-nanowire HTD PD SOI n-MOSFET. The voltage swing is much better than any other device because of large constant saturated drain current. The HTD MOSFET has less doping, high gain and large cutoff frequency.

2. DEVICE STRUCTRURE AND SPECIFICATION

A. Device structure of nano length Ge based tunnel diode

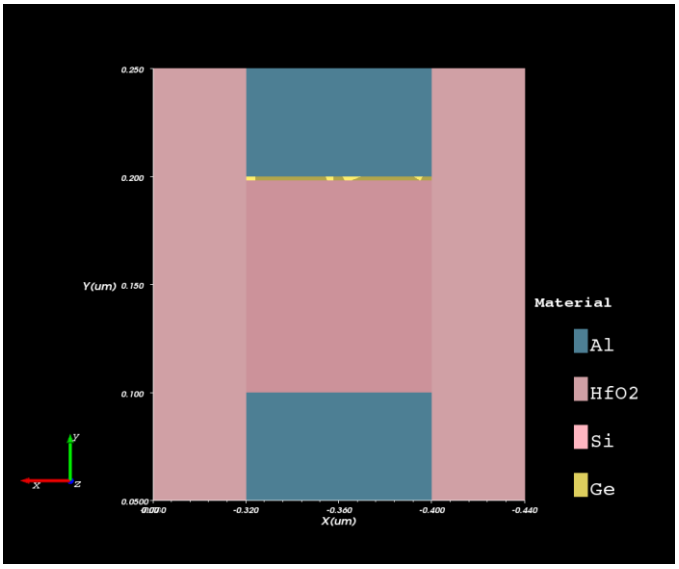

Figure1: Device structure of Ge-nanowire HTD.

The device shown in figure 1 is simple heterojuction architecture of Ge on Si material. This is a 2-Dimensional model formed on the Visual TCAD. Firstly, a simple Si substrate of length 0.1 um and width0.08um was taken and then it was doped with donor impurity of concentration 7.5×10^{18}. Afterwards, intrinsic Ge nanowire of varying thickness from 2-10 nm has been merge on the top of the Si layer. The device is shielded by layer of HfO_2, which reduces the leakage current of the HTD.

B. Device structure of embedded tunnel diode based N-MOSFET

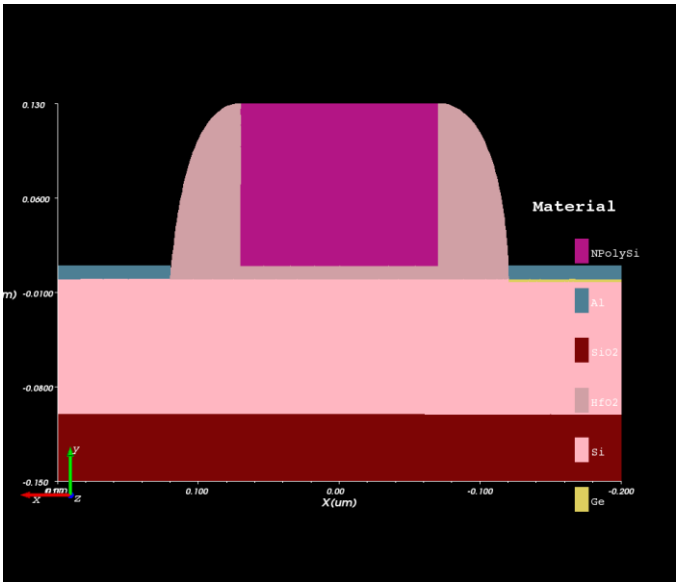

Figure 2: Device structure of the nanowire Ge HTD *n*-MOSFET

Figure 2 shows the device structure of the HTD PD SOI *n*-MOSFET. In conventional SOI *n*-MOSFET the source region consist of a single layer of Si substrate. Here, in HTD PD SOI *n*-MOSFET the source region is replaced by the Heterojunction Tunnel Diode which consist of the Si and Ge layer of thickness 0.08um and 0.02um respectively. The SiO2 layer used in the base of Si layer is of thickness 0.1um. The gate material used in a proposed structure is an N-polysilicon which has work function of 4.71eV. The gate oxide thickness is kept at 1.5nm so as to avoid tunnelling of electron and hole from channel to gate.

C. Principle of Device Operation.

In proposed structure, heterojunction tunnel diode is used to enhance the electron flow from source region to drain region. The recombination current dominates the total current at low forward bias because of the heavy holes flow from intrinsic Ge region to silicon region inside source region. The current obtain from this tunnel diode combination is constant at low forward bias region shown in figure 4.

III. Device Simulation

Extensive device simulations were performed using Cogenda device simulator coupled with analytical calculation. These device simulators are based on drift diffusion model and physical device model and consider the effect of mobility, Shockley-Hall-Read and Augur recombination etc. The operation of the heterojunction tunnel diode based N-MOSFET based on the principle of band to band tunnelling using hurkx model [9]. As shown in figure constant increased drain saturated current is obtained in the proposed device without increasing the gate voltage which is better for analog application than any conventional PD SOI *n*-MOSFET structure.

IV. Experimental Results and Discussion

In order to study, the heterojunction tunnel diode behaviour in terms of I-V characteristics, Transconductance behaviour and frequency response. Figure 3 shows the current-voltage (I-V) characteristics of heterojunction tunnel diode taken at room temperature showing pronounced negative differential resistance (NDR) with PVR of 2.8 at a very low voltage of 0.5V. It is shown that the current increases to a maximum peak current (I_P) at a peak voltage V_P in the forward bias.

It was found that variation of I-V curves at varying germanium lengths from 2nm to 10nm. The PVR increases as the germanium length decreased from 2nm to 10nm length, with the highest peak valley ratio of 2.91. The current in this region can be computed from equation 1 [12].

$$I = Ip\frac{Vin}{Vp}e\left(1-\frac{Vin}{Vp}\right)+Itho[\exp\left(\frac{Vin}{nkT}\right)-1] \qquad (1)$$

Where Vin is the voltage across the heterojunction, Ip is peak current and Vp is peak voltage, Itho is the saturation current for thermionic emission, and n is the diode ideality factor. The calculation shows that the maximum current obtained from equation, which matches with the simulated results also.

It was noticed that the sharp peak current was obtained at 2nm Ge length is 3.90e-06A, the peak voltage of 0.1 V and the valley current is 1.97e-06A. It was also found that, as the Ge width was increased from 2nm to 3nm, the peak current has reduced from 3.90e-06A to 2.39e-06A and also the valley current is reduced from 2.39e-06A to 1.41e-06A. The reason behind this drop is that, as the Ge width is increased from 2nm to 10nm the mobility are degraded due to hole accumulation. For this cause NDR region is decreased hence device switching is slow.

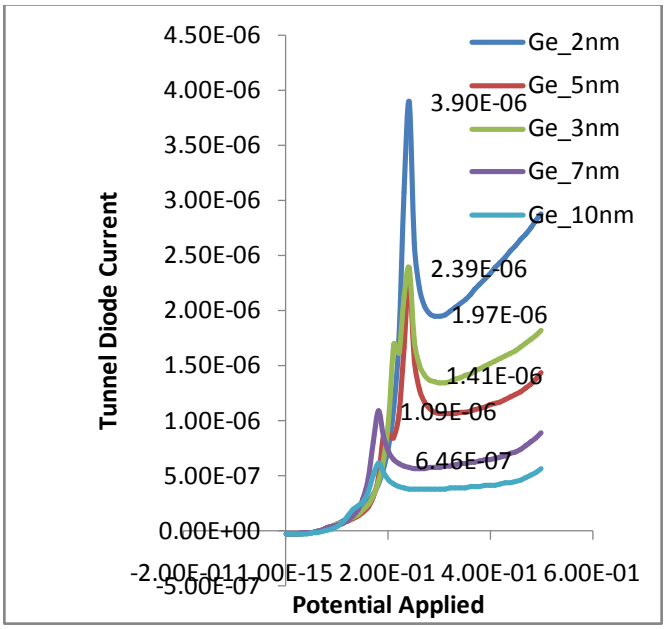

Figure.3: I-V characteristics of Ge nanowire HTD were Ge width is vary from 2nm to 10nm.

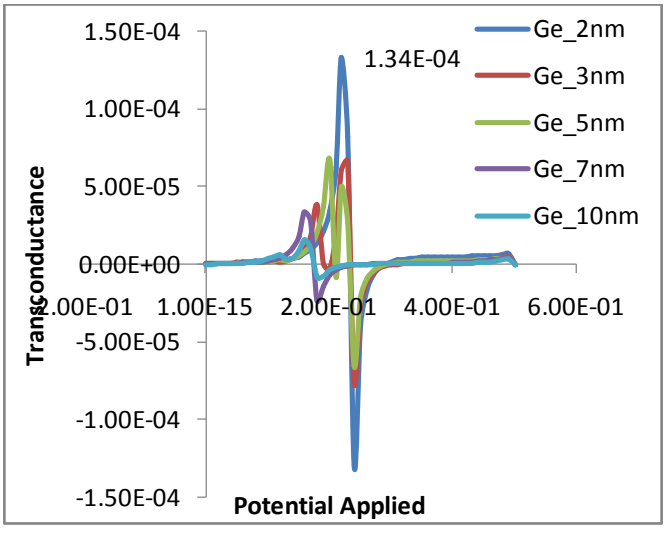

Figure.4: Transconductance curve with the anode potential of HTD at different Ge layer thickness from 2nm to 10nm.

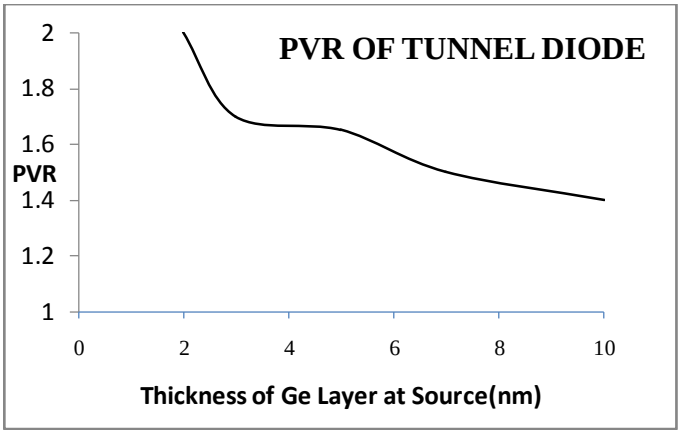

Figure.5: Peak to valley ratio of embedded tunnel diode in proposed MOSFET with varying Ge-layer thickness from 2nm to 10nm.

In order to study the frequency in HTD the transconductance parameter play an important role. To investigate the frequencies of the HTD in greater detail plot the curve between $\frac{\partial I}{\partial V}$ vs varying anode potential.

Figure5 shows the curve between transconductance and varying anode potential of the HTD. It was found that highest positive peak current obtained at the Ge_2nm width is 1.34e-04, similarly negative peak current is obtained at all Ge naometer width. As the Ge width is increased the transconductance was decreased due to low NDR region.

Figure 6 shows the curve between Peak to valley ratio of embedded hetero junction tunnel diode with varying Ge layer thickness from 2nm to 10nm. The maximum PVR is at 2nm Ge layer thickness in source region, as the thickness is increased the PVR are decreased.

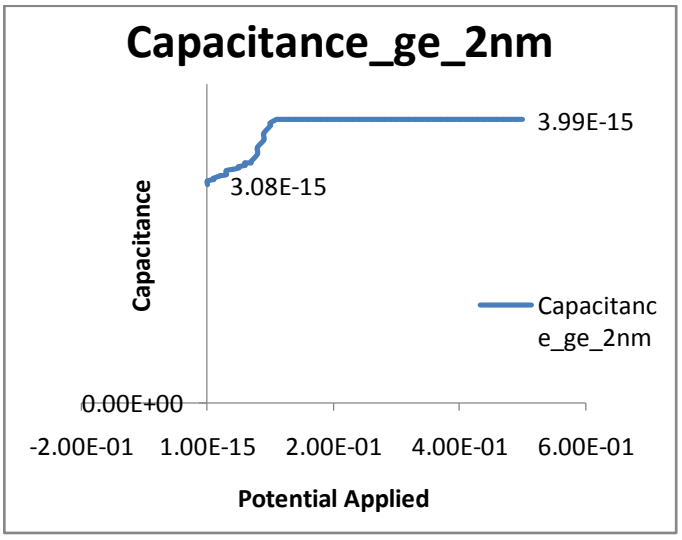

Figure6: Measured gate capacitance characteristics of the HTD at 2nm Ge-layer thickness in source region.

Figure7 shows the curve between maximum capacitance and varying anode potential from 0 to 0.5 V. It was found that the

maximum capacitance at 2nm Ge layer thickness is 3.99 fF which is constant for all anode voltage. The operating frequency of tunnel diode is computed by equation 2.

$$Ft = \frac{1}{2\pi C}\left(-\frac{gm}{ro} + gm^2\right) \qquad (2)$$

Where, C is capacitance, ro is output resistance and gm is transconductance. Hence by putting all the value the cut-off frequency of tunnel diode is 12 GHz which helps to increase the cutoff frequency of MOSFET for RF application.

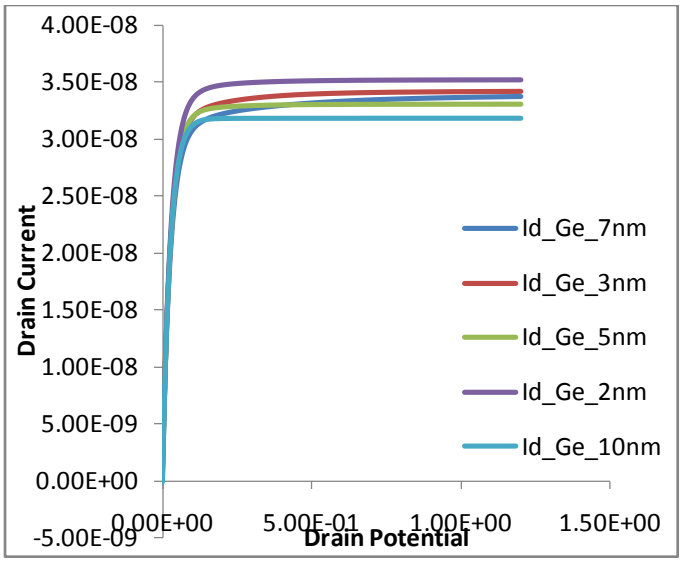

Figure.7: Output characteristics of the HTD n-MOSFET with a gate length of 0.10um. Kinks are suppressed in the proposed at different GE width in the source of HTD MOSFET structure

In order to implement the above characteristics of HTD in MOSFET structure, the different parameters are studied such as output characteristics, voltage swing and frequency behaviour of proposed MOSFET. Figure8 shows the output characteristics of proposed MOSFET for varying thickness of Ge nanowire layer at source region. In the conventional PD SOI-MOSFET the kink phenomenon appeared due to the hole accumulation in the p-body. The impact ionization occurred due to these holes that raises the bodypotential and reduces the threshold voltage resulting increased linearly of drain current in saturation region [11]. It was found that in figure 7 no kink phenomenon is obtained in the proposed Ge-nanowire HTD PD SOI *n*-MOSFET structure.

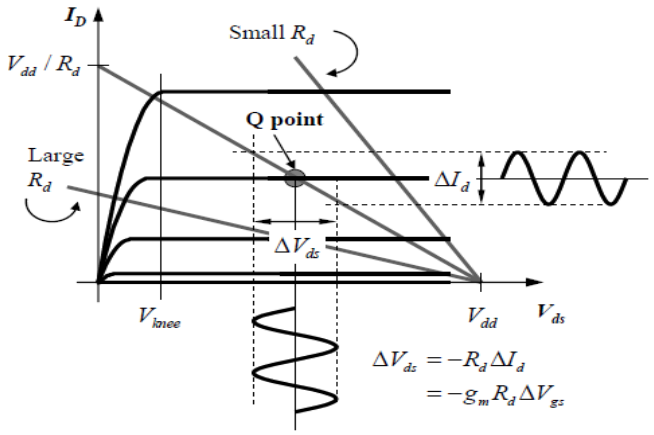

Figure8: Id vsVds curve of Typical MOSFET which shows the constant saturated current give the 95% of voltage swing at output [11]

Figure8 shows the output characteristics curve for ideal MOSFET.It is shown that constant saturated drive current gives the maximum voltage swing. It has been observed in the proposed HTD PD SOI-MOSFET structure from figure 7, the constant saturated drain current was found at very low 0.3V drain voltage, hence get large voltage gain and swing.
Figure 7 shows that maximum drain current was obtained at high Peak to valley ratio of embedded tunnel diode when Ge layer thickness is 2nm in the source region. As the width of Ge is increased the drain current was decreased. And it is also says that if PVR of tunnel diode is decreased the drain current is also decreased because the high NDR region is obtained at Ge_2nm hence tunnelling of electron more in this region so the drain current is increased.

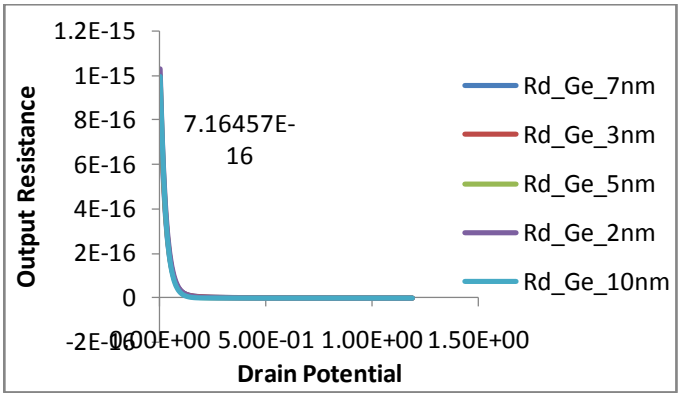

Figure 9: Output resistance curve with respect to drain potential at different Ge width in HTD-MOSFET for getting high voltage gain.

In practical analog application of the hetero junction tunnel diode based N-MOSFET the distortion is reduced due to high constant drain current was obtained and hence get large voltage swing and sustained oscillation. The HTD PD SOI *n*-MOSFET provides a high voltage gain due to high output resistance

shown in Figure 10. The gain of the MOSFET is high by given formulae

$$Av = -Gm\ Rd \qquad (3)$$

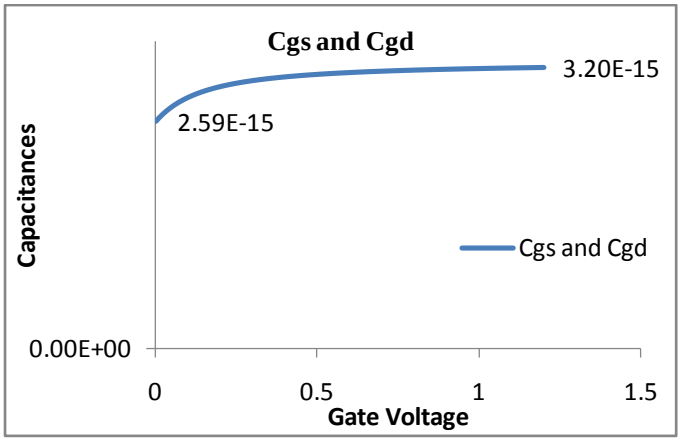

Figure 10: Measured drain and gate capacitance of the HTD-MOSFET at different gate voltage

In the high speed digital applications, cutoff frequency Ft is an interesting criteria, which transit the frequency of the current gain. The cutoff frequency of MOSFET is

$$Ft = \frac{Gm}{2\pi(Cgs + Cgd)} \qquad (4)$$

Where, Cgs is the gate to source capacitance, and Cgd is the gate to drain capacitances. The gate capacitances are measured out an HTD n-MOSFET. The result is shown in figure when Vg is varying from 0 to 1.2V, the gate capacitance of HTD MOSFET is 3.20 fF. Hence it is shown that the HTD PD SOI *n*-MOSFET is more practical application then the normal *n*-MOSFET, the cutoff frequency of HTD MOSFET is 2GHz frequency which is useful for microwave devices.

V. Conclusion

In this paper proposes a possible solution that can suppress the kink effect of conventional PD SOI *n*-MOSFET by means of a new type of device, which is referred as the Ge-nanowire HTD PD SOI *n*-MOSFET. The voltage swing is 90% improved than any other SOI MOS devices because of large constant saturated drain current. The proposed HTD MOSFET structure gives maximum drain current at 2nm Ge layer thickness. The embedded tunnel diode in Proposed MOS structure have high PVR of 2.91 and cutoff frequency of 12 GHz at 2nm Ge layer thickness which help to increased the cutoff frequency of proposed MOSFET that is equal to 2GHz. The proposed structure are helpful in RF and low power digital and analog application.

Acknowledgement

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