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Probabilistic Activity Estimator and Timing Analysis for LUT Based Circuits

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Abstract— Low power VLSI has received tremendous attention due to power constraints in designs. This paper details a survey on switching activity estimation techniques. It also presents a computationally efficient activity estimator which is probabilistic in nature. This estimator is faster and accurate. Simulation based approach is practically impossible for large circuits. More statistical parameters related to activity estimation are incorporated to improve the accuracy. This methodology is implemented on MCNC benchmarks. LUT mapping is done using the logic synthesis tool ABC. Spatial correlation is considered by computing the activities at each LUT. Power estimation using Synopsys Design Compiler tool gave 18% reduction in dynamic power for optimized circuits. Timing analysis plays an important role in circuit design. Statistical Timing Analysis (STA) is performed and the delay analysis is obtained. An effective tradeoff between timing and power were reported.

Keywords - estimation, simulation, field-programmable gate arrays (FPGAs), probabilistic, Look Up Table(LUT).

I. Introduction

Digital circuits can be implemented basically on FPGA platforms. Power consumption increase of ICs is a major concern in semiconductor industries. This along with three low power design techniques namely voltage scaling, technology scaling and reduction in node activity capacitance are considered in general for any design [1].Field Programmable Gate Arrays(FPGAs) are less power efficient than ASICs. Activity estimation and minimization are taken into account for reducing the dynamic power in FPGAs. Any work that focuses on low power specifies which CAD tool to minimize power[2]. Power consumption of a CMOS circuit [3] was determined using methods like probabilistic approach. At an average minimal speed up was reported but gate input correlations were not considered. Glitch power estimation [4] is taken into account and transition probabilities were well explained for real delay models. Uncorrelated inputs and correlated inputs were related with real delays and validated. A variety of circuit techniques are explored in[5] for reducing the leakage power in submicron devices. Leakage power is highlighted more so as its effects are predominant in devices. Accurate power estimation is needed for optimization [6] and it should be fast. Exact computation and approximate computation are carried out for large circuits. System level and design level techniques are elaborated in [7] and it focuses on applications which require high energy and power. Transition density [8] concept applies well to node switching activity and its propagation from primary input to internal nodes and output are well correlated.

A detailed survey of power estimation techniques presented in [9] covers signal probability apart from transition density. Spatial and temporal correlations along with a Binary Decision diagram representation and simplified delay models are used. It concludes that statistical approach gives a mix of speed and accuracy.

FPGAs have LUTs, configurable logic blocks and routing pads as basic units. It dissipates two types of power namely static and dynamic. The dynamic power consumption is a major factor which depends on internal signal transition [10].This work concentrates more to estimate these transitions to calculate the switching activity. Also STA is carried out and the results gave an over all delay analysis pertaining to the topology. Node activity and switching are to be determined well before power modeling as they are treated as serious issues. An abbreviated version of this paper was published in IJERA[21].

This paper is organized as follows: Section II draws the basics on switching activity measures. Section III presents an overview of existing activity estimation techniques and STA. Section IV includes the methodology. Section V discusses the experimental results and Section VI offers the conclusion.

II. Basic Terminologies

Any activity estimation technique for industrial applications should consider correlation as an important measure .It may be spatial correlation, temporal correlation, spatio-temporal dependencies, circuit delays and glitches.

A Spatial Correlation

The relation between input signals of a gate determines the spatial correlation . This correlation happens due to logical value dependence of a wire on another wire.. It can also occur at the primary input of the gate and there may be chances that when gates branch out .This branch out gates later reconverge. This is depicted in figure 1. Signal A generates two signals namely C and F. Hence Signal A can be termed as the parent signal of C and F. The output level (high or low) of C is related with the probability of signal F being high or low. Mutual dependency plays an important role in determining the static probability of a signal.

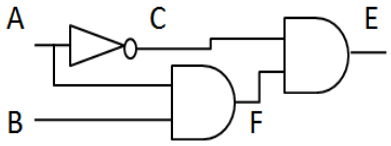

Fig.1. Example for spatial dependency of signals

B Temporal Correlation

When the node value depends on its previous value temporal correlation is said to exist. This mainly occurs in circuits having feedback and it may also occur at the primary input .Ignoring this correlation may lead to a huge error.

C Spatio-Temporal Dependencies

This measure considers time as a metric and estimates the relation between the output and input .It observes the behavior of output signal to the input over a period of time. This type of dependencies are common in circuits like sequence generator

D Circuit Delays and Glitches

Glitch occurs in a circuit when a logic gate encounters delay. In the circuit shown in figure 2 a transition occurs from 00 to 11.An intermediate transition occurs before the output settles to a stable value which is termed as glitch. When the input state changes, transitions are generated in a LUT. Difference in the arrival times of input may generate glitches. It is depicted in figure 3.

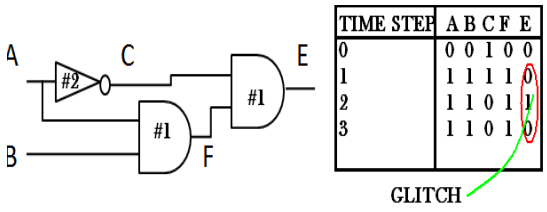

Fig. 2. Glitch generation in a circuit due to gate delays

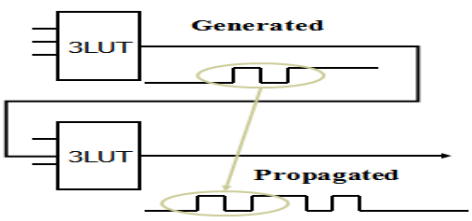

Fig.3. Glitches generation and propagation in LUTs

III. Existing Activity Estimation Techniques and STA

The existing gate level probabilistic techniques to model the power estimation was modified in [11] at dual instances. This had an improvement in consistent power estimation. Power estimation related to transition density, consideration of glitches, modelling of dependencies were reported in [12-13].Linear decomposition and synthesis [14] dealt with xor based logic circuits and their comparison with the existing tools ABC and BDS –PGA 2.0.Modern ICs in nanometer technologies face time and power issues along with process variations. Onchip variations are common and their focus with respect to statistical static timing analysis [15] has proven worth for a long range.

The details on the logic synthesis tool ABC[16] and BLIF benchmarks [17] presented a great impact for this work. The recent work in the field of probabilistic power estimation was using the technique described in [10]. Various factors like delays, glitches and correlation were considered. Also an xor based decomposition method was employed to the circuits. This method works well for small range circuits. For large input circuits this approach fails.

Static Timing Analysis is a method for analyzing and computing delays for digital circuits. It is advantageous over the vector based timing simulations. A conservative analysis of the delay can be given by STA. Timing variation issues are dealt clearly in [18].This method has been applied to level sensitive latches and in the presence of cross talk [19].STA predominantly checks for setup and hold violations. Slew propagation at the gate level analysis [20] predicts all variations to be in a finer range.

IV. Methodology

The basic problem formulation is listed in the steps below.

i) Map the circuit into LUTs
ii) LUT traversal is treated as a graph traversal problem
iii) Circuit in each LUT is treated as a directed graph
iv) Convert real input vectors to equivalent statistical quantities
v) Statistical approach is carried out for power estimation to obtain the statistical parameters
vi) Propagate statistical parameters through the circuit.
vii) Compute activities of every node.

A probabilistic switching activity estimator is presented and compared with a simulation based activity estimator. A comparative study with other existing probabilistic activity estimators is also performed. Figure 4. describes the methodology. Microelectronic Center of North Carolina circuits(MCNC) in BLIF (Berkeley Logic Inter Changeable Format) were used for validation . The results are compared using a simulation based activity estimator and existing switching activity estimators like ACE v2.0 academic tool produced from the University of British Columbia, Vancouver, BC, Canada , Synopsys DC compiler and commercial Quartus II 9.0 CAD tool.

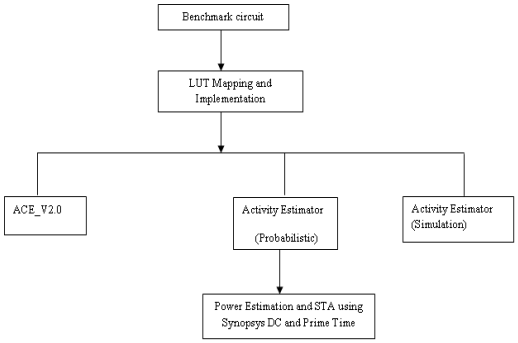

Fig.4. Methodology

The Altera Stratix II FPGAs which utilize four input LUTs are considered. The benchmarks are LUT mapped using the tool ABC. Conditional probabilities define the relation between static probabilities of logic functions. The probability values obtained due to correlation are propagated to the output.The effects of spatial dependencies were checked by providing correlated samples as inputs. It was from an audio file. Testing was carried out using the samples generated from MATLAB. Static probability and switching arte of input vectors were determined. The data is fed to the proposed simulator. The programming is done in C language. Power estimation is done using the Synopsys Design Compiler and the timing is carried out using the Synopsys PrimeTime. STA was performed to give a general tradeoff between the power and timing.

V.Results and Discussion

The experiments are performed on MCNC benchmarks. Comparison with the simulation based approach is carried out and the variation is reported for basic circuits. The equivalent statistical information is used for the proposed switching activity estimator. Table I reports the comparison on simulation and probabilistic switching activity estimation for basic circuits.

Table I. Comparison of activities from simulationbased and probabilistic switching activity estimators (tc: toggle count, s.p.: static probability)

Circuit	Simulation based Approach		Probabilistic Approach (proposed)		Relative Error %
	T.C.	S.P.	T.C.	S.P.	
Half Adder	637	0.4243	909	0.3371	30
Full Adder	746	0.4973	2060	0.4333	64
4:1 mux	747	0.4980	1155	0.4153	35
2:4 decoder	331	0.2208	834	0.6185	60
BCD-EX3	705	0.4698	986	0.5200	28

Consider a full adder circuit the toggle count is greater when compared to the toggle count of 4:1mux in probabilistic approach. It is compared with the simulation based approach. The relative error show vast variation between the two methods. Table II and Table III shows the simulation results for the BLIF benchmark circuits in Quartus II 9.0sp2 and Ace_v2.0.The dynamic power shows an increase with respect to the number of logic elements. The switching probability and static probability values also show a remarkable trend in this estimation. For the circuit pair the static probability shows a higher value and it is due to its logic structure.

Table II. Simulation Results For The BLIF Benchmark Circuits In Quartus II 9.0sp2

Circuit	Logic elements	Dynamic power(mw)	Static probability	Switching probability
ex5p	198	13.05	0.938600	0.472312
i8	265	14.76	0.976542	0.4873410
misex3	893	57.48	0.227102	0.346351
Pair	325	15.96	0.982310	0.397854
Seq	1033	71.77	0.708942	0.480792
table3	247	13.90	0.884640	0.396531
x3	161	12.45	0.893124	0.412953

The number of critical path elements are calculated and reported in Table III.T he number of inverters is found to be high in the circuit seq. It has more number of critical path elements and the time required for traversal is high.

Table III. Bench Mark Circuit Details : Ace_V2.0

Circuit	Input/ Output	OR Gate	AND Gate	NOT Gate	No. of critical path elements
ex5p	8/63	1779	3187	3558	15
i8	133/81	430	1029	1294	9
misex3	14/14	2552	3398	5114	13
Pair	173/137	669	1391	1815	14
Seq	41/35	2939	4081	5878	25
table3	14/14	337	776	1052	12
x3	135/99	312	689	946	7

Table IV shows the optimized and LUT details using ABC tool. Dynamic power dissipation from Synopsys DC is shown in Table V. A significant amount of reduction was obtained for optimized circuits. ABC is a LUT mapper tool. For the optimized circuit the number of edges, and or inverter graphs and number of critical path elements were calculated .The number of critical path elements reduced in all cases as we have selected 4 input LUTs for mapping.

Table IV. Bench Mark Circuits Details(Optimized And Lut Mapped) : ABC Tool

OPTIMIZED				LUT MAPPED		
Circuit	AND Gate	No. of critical path element	No. Of LUTs	Edge	AIG	No. of critical path elements
ex5p	1460	14	790	2560	1885	7
i8	811	12	332	1225	929	5
misex3	2142	12	1088	3688	2763	6
Pair	1231	18	475	1627	1442	7
Seq	2412	12	1235	4122	2989	6
table3	636	13	321	1074	766	7
x3	582	12	219	762	630	5

Table V. Power Estimation: Synopsys DC Tool

Circuit	Dynamic power (µw)		
	Original Circuits	Optimized Circuits	LUT mapped
ex5p	94.8591	104.3925	107.0862
i8	93.9305	94.0193	95.4144
misex3	224.4607	213.8829	214.7013
Pair	192.3651	187.4321	185.2300
Seq	256.6752	254.1298	255.8760
table3	48.0066	45.7881	45.7794
x3	81.9852	72.8221	75.1287

Dynamic power estimation using Synopsys DC tool gave an overestimate for few cases. The value obtained for general cases revealed up to 18% reduction in power.

Table VI . Results On Application Of Random Input

Circuit	Proposed simulator	Synopsys	ACE v_2.0
ex5p	0.0871	0.0085	0.0607
i8	0.0033	0.0053	0.0098
misex3	0.1326	0.0466	0.1111
Pair	0.0017	0.0048	0.0055
Seq	0.0039	0.0076	0.0347
table3	0.0669	0.0529	0.0512
x3	0.0187	0.0286	0.0050

From table VI it is evident that on applying random inputs the proposed simulator gave significant results. For the set of correlated inputs the response is given in Table .VII. It is evident from table VII that when correlated data is fed as input the toggle rate estimation error varies according to the type of the simulator.

Table VII . Results On Application Of Correlated Input

Circuit	Proposed simulator	Synopsys DC
ex5p	0.0714	0.2243
i8	.0012	0.8265
misex3	0.2214	1.3585
Pair	0.0023	0.6085
Seq	0.0026	2.3106
table3	0.0779	3.9726
x3	0.0793	3.4232

The values show a nominal response for these inputs. STA is performed on the same set of circuits and the response is tabulated in table VIII. Since each logic has large elements a one unit clock period is not sufficient to drive the entire unit and hence a negative slack is obtained. When the clock value is slightly increased to 5units a positive slack is obtained. Since wire delays and gate delays are ignored this value of slack is not precise. For a precise timing estimate Statistical Static Timing Analysis can be used.

Table VIII. STA To Find The Worst Case Delay

Circuit	Inputs	Outputs	Slack when Clk=1unit	Slack when Clk=5unit
ex5p	8	63	-1.49	2.51
i8	133	81	-1.13	2.87
misex3	14	14	-1.46	2.54
pair	173	137	-1.41	2.59
seq	41	35	-1.65	2.35
table3	14	14	-1.38	2.62
x3	135	99	-0.66	3.34

VI. Conclusion

This paper examined several switching activity measures. Their advantages and disadvantages were listed. In general an activity measure and timing measure were suggested for LUT based circuits.STA results were found to be pessimistic for design analysis. So providing more statistical information pertaining to each and every node on the circuit and analysis can be made. Statistical Static Timing Analysis can be carried out. Also usage of an algorithm for LUT traversal may improve the processing time and this approach can also be generalized to applicable for all FPGA architectures which can be incorporated as future scope of this work.

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