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Design of Low Power High Speed SRAM Cell

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Abstract- Static Random access memory (SRAM) are useful building blocks in many applications such as a data storage embedded applications, mobile applications, which are in demand for low power and high speed operations. In this paper an efficient implementation of 9T SRAM cell using Multi Threshold voltage CMOS (MTCMOS) technique is proposed for improving high performance even at low power. A 256 bit memory array is designed using 9T SRAM cell based on MTCMOS technique. The memory array has been designed, implemented & analyzed in standard 130nm technology library using Mentor Graphics Pyxis Schematic Editor.

Keywords: Multi Threshold CMOS (MTCMOS), High Threshold Voltage (HTV), Low Threshold Voltage (LTV), SRAM, PMOS, NMOS, V_{TH}

I. Introduction

Now-a-days many micro-watt applications, such as data storage embedded electronics; implantable biomedical devices, mobile applications etc are evolved. They play a prominent role in minimization of power consumption to prolong battery life. However, design of ultra low voltage digital and memory circuits is highly required for achieving low power consumption and high speed. In any conventional CMOS circuit, the total power consumption is described as the sum of dynamic and static power throughout the operation of the circuit. When the circuit is in standby mode, leakage power is dominant. Dynamic power consumption is classified into two types. The switching power is contributed for charging and discharging of load capacitance. Hence, to restrain the power consumption in critically low-voltage circuits, it is needed to reduce the leakage currents in standby modes of operation [1]-[3].

Many research works have been conducted for reducing SRAM power consumption. The research on the utilization of MTCMOS is of huge interest. In order to reduce the power consumption, operating voltage (V_{DD}) is positioned near or below threshold voltage (V_{TH}), known as sub-threshold region. In MTCMOS technique Low Threshold Voltage (LTV) CMOS is required to increase the performance of the device and High Threshold Voltage (HTV) CMOS is required to reduce power consumption of the device. As a result, the leakage currents are significantly reduced in both the standby and active modes compared to all LTV implementation. At the same time, circuit performance

is maintained at low supply voltages. MTCMOS requires two extra transistors (PMOS &NMOS) which are operated in high threshold voltage region for reducing leakage current . As a result MTCMOS technique occupies more area. These are known as sleep transistors. Sleep transistor require high threshold voltage hence by changing the body bias voltage will get high threshold voltage transistor.

The threshold voltage of a transistor can be calculated as follows

$$V_{th} = V_{fb} + 2\varphi_b + \frac{\sqrt{2\epsilon_{si} q N_a (2\varphi_b + V_{sb})}}{C_{ox}}$$

Here V_{fb} represents the flat band voltage,φ_b is the built in potential, V_{sb} is substrate bias voltage, C_{ox} is the oxide capacitance, N_a is the acceptor concentration.

The conventional 6T SRAM cell and The SRAM cell using dynamic threshold voltage technique are described in section II, and the proposed SRAM cell using MTCMOS technique are described in section III and 256 bit SRAM memory array is described in section IV. The simulation results for all the designs implemented using Pyxis Schematic Editor 130-nm technology are discussed in section V.

II. Preliminary Concepts and Previous Work

A. Conventional 6T SRAM Cell

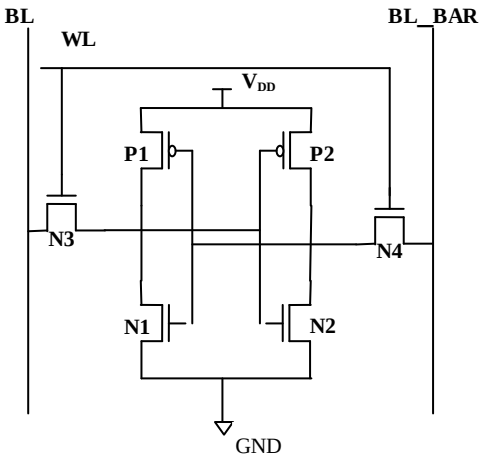

Fig .1 6T SRAM cell

Conventional 6T SRAM cell works on the full voltage swing. This says that if the operating frequency of the SRAM cell is increased then the dynamic power dissipation will also be increased. Hence, for high speed CMOS operation the conventional 6T SRAM [4] cell is not a good choice. And also data read and write operations are happening correctly with some leakage power. In SRAM there are two short circuit leakage paths, one is from supply voltage to ground and another one is from bit line to ground. Therefore both leakage paths are discharging to ground.

B. SRAM cell using dynamic threshold voltage CMOS

SRAM Cell includes the benefits of Dynamic threshold voltage control scheme [5] to reduce leakage energy. SRAM cell which is not accessed for a certain time period will be assigned high V_{th} and reduces stand-by voltage, and SRAM cell which is in frequent use will be assigned low V_{th} and normal V_{DD}. Dynamic threshold voltage scheme significantly reduces leakage power but its performance gets reduced due to memory wakeup delay.

III. Proposed SRAM cell Design

A. MTCMOS Technique

Low-power and high speed SRAM cell can be achieved by using MTCMOS technique. This technique uses low and high threshold voltage transistors are used in single chip only.

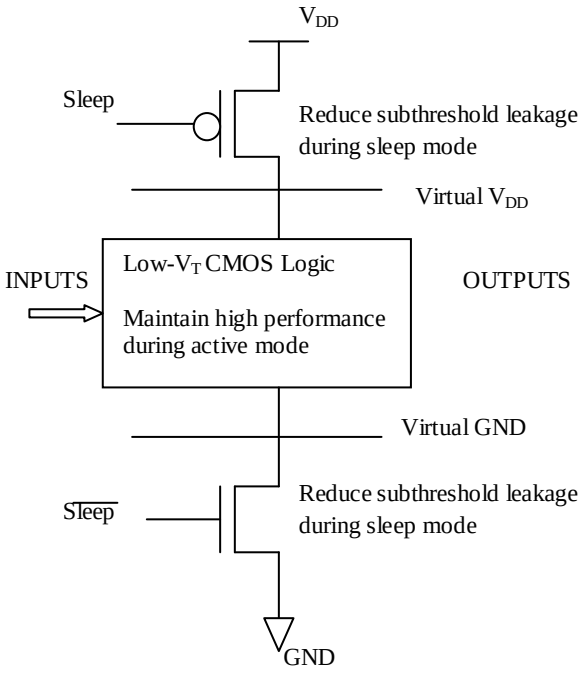

Fig. 2 MTCMOS Circuit using sleep transistors

Low threshold voltage transistors which have high Performance is used to reduce the propagation delay in the critical path during active mode. High threshold voltage transistors which have less power consumption are used to reduce the power consumption in the shortest path during sleep mode.

Multi threshold voltage CMOS reduces leakage current by adding high V_{TH} devices in series with low V_{TH} .Figure 2 represents the block diagram of MTCMOS circuit. A sleep control scheme is introduced for efficient power saving method. Sleep is set low and sleep control high V_{th} transistors are turned on in the active mode of operation. Since their on resistances are small, the virtual supply and ground voltages almost as a real power lines. Sleep is set high, both NMOS and PMOS transistors are turned off, and the leakage current is low.

B. Conventional 9T SRAM cell

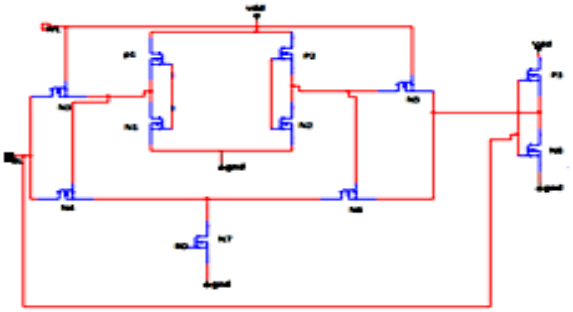

Fig. 3 9T SRAM cell

The 9T SRAM [8] is shown in Figure 3. Write operation occurs as in that of 6T SRAM cell. Read operation occurs separately through N4, N6 and N7 controlled by the Read Signal RD going high. This design has the problem of the high bit line capacitance with more pass transistors on the bit line and it can be reduced by placing sleep transistors on bit line.

C. Design of 9T SRAM Cell Using MTCMOS Technique

Operation of 9T MTCMOS SRAM cell is same as that of conventional 9T SRAM cell, which is having more power dissipation because of high bit line capacitance due to more switching transitions at bit line node. It can be reduced by placing high threshold transistors (PMOS & NMOS) between supply and ground, so that the unwanted and more transitions can be decreased by controlling switching transistors (low V_{th} and high V_{th}) which are placed in between power supply and ground. So that power consumption and delay both are reduced in a single circuit.

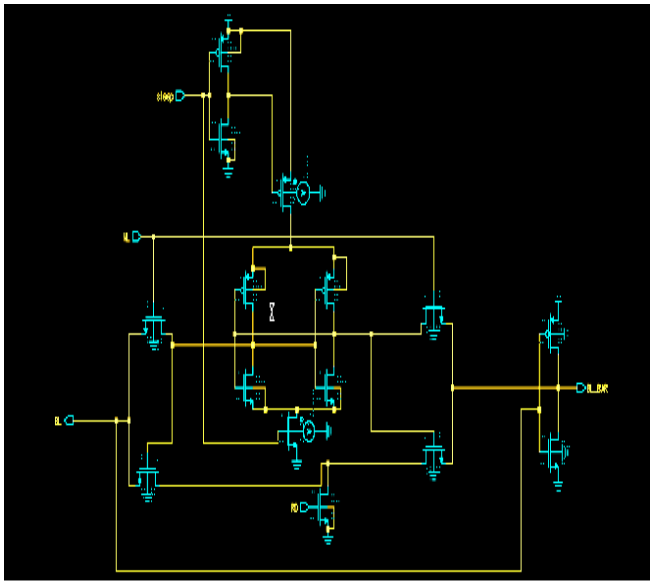

Fig.4. SRAM cell using MTCMOS Technique

D. Design of SRAM Cell Using MTCMOS Technique with read and write operations

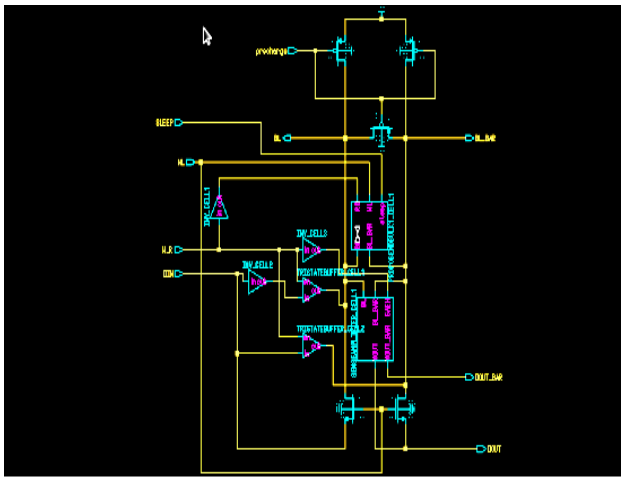

Fig 5 SRAM cell during write and read operations

IV. 256 Bit SRAM Array Design

The 16x16 memory array is capable of storing 256 bits. It consists of 256 bit SRAM cells, 16 sense amplifiers, 16 precharge circuits, one 4×16 row decoder, one 4×16 column decoder, 16 write driver circuit. As the capacity of SRAM cells increases the sizing of the transistors changes due to loading effect. Each column has a single sense amplifier, write driver circuit, pre-charge circuit.

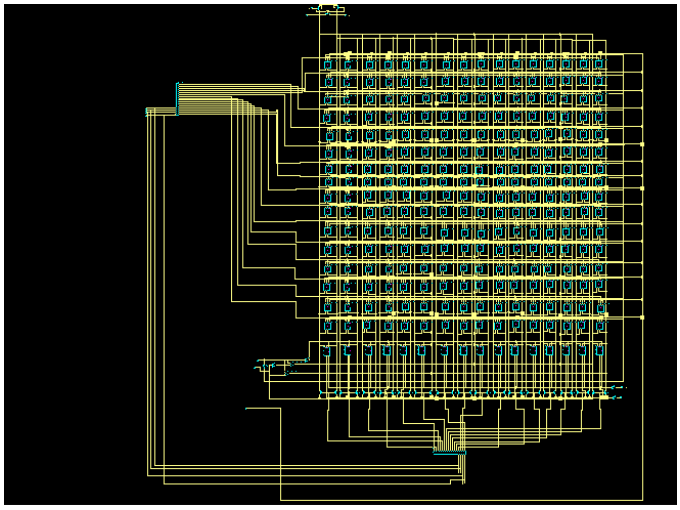

Fig.6 The 256 bit SRAM memory array

V. Results and Comparisons

The power consumption, delay and power delay product of the proposed SRAM cell design using MTCMOS technique are evaluated against the SRAM design using dynamic threshold voltage technique.

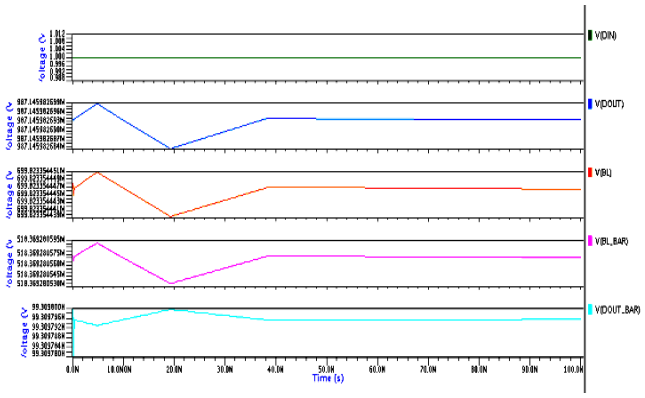

Fig. 7 Simulation result of read logic 1 operation using MTCMOS

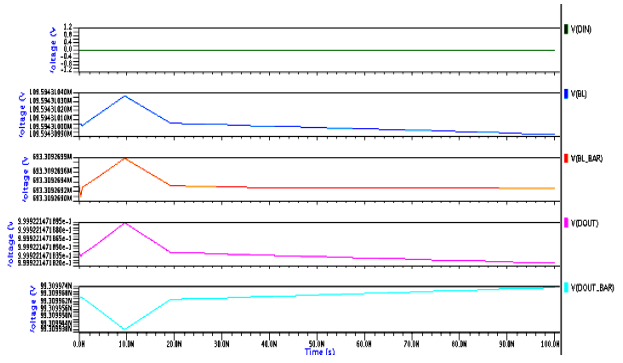

Fig. 8 Simulation result of read logic 0 operation using MTCMOS

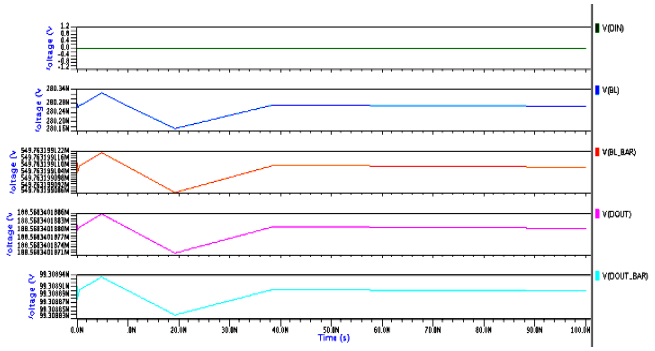

Fig. 9 Simulation result of write logic 0 operation using MTCMOS

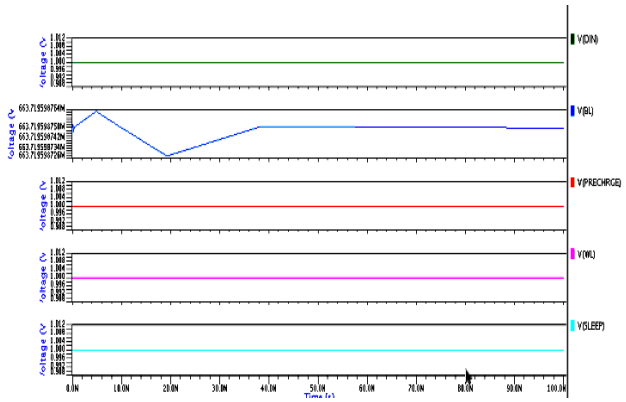

Fig. 10 Simulation result of write logic 1 operation using MTCMOS.

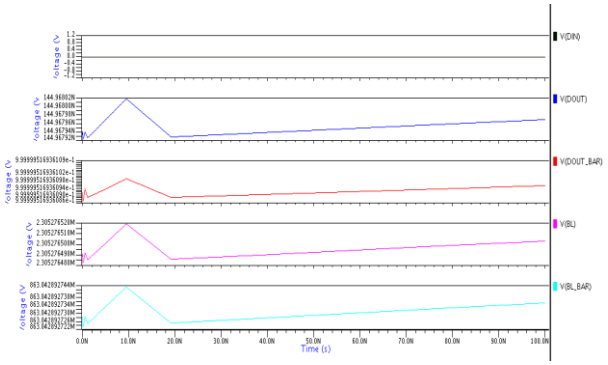

Fig 11 simulation results of read logic 0 operation for 256 bit SRAM array.

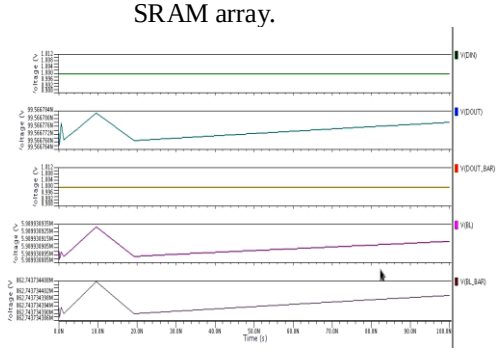

Fig 12 simulation results of read logic 1 operation for 16×16 SRAM array.

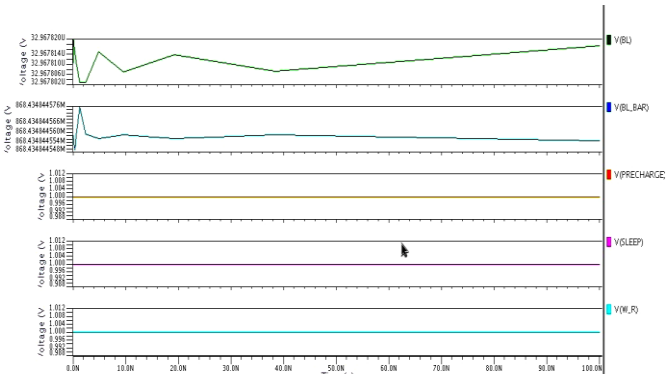

Fig 13 simulation results of write 0 for 16×16 SRAM array

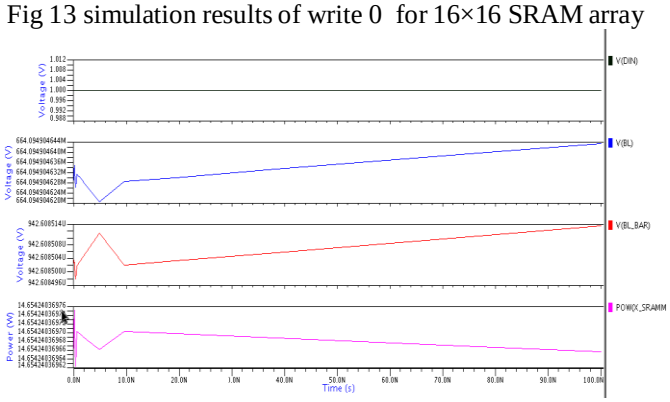

Fig 14 simulation results of write 1 for 16×16 SRAM array

The compared designs include read and write operations for both logic levels. The target technology is the Mentor Graphics Pyxis Schematic Editor 130-nm technology.

The following TABLE I show the read and write operations for both DTCMOS and MTCMOS Techniques. Analysis has been done for the following parameters such as Power, Delay and Power delay Product .SRAM using MTCMOS Techniques has given better results compared with SRAM using DTCMOS.

TABLE I **Simulation results of SRAM Cell in 130nm/27^{0}c at V_{DD} =1V**

Operation	**SRAM using DTCMOS**			**SRAM using MTCMOS**		
	Power (mw)	**Delay (ps)**	**PDP (pws)**	**Power (mw)**	**Delay (ps)**	**PDP (pws)**
Write 0	73.35	48.35	3.546	57.68	30.86	1.79
Write 1	73.39	219.61	16.11	57.44	214.41	12.88
Read 0	75.56	139.30	10.53	58.09	33.52	1.947
Read 1	75.22	450.52	33.89	57.89	244.32	14.14

By using SRAM with MTCMOS technique the power dissipation for both write 0 and write 1 operation is reduced by more than 21%. For read 0 and read 1 the power is reduced by more than 23%. For delay with write 0 it is reduced by 36%, write 1 it is reduced by 3%, in the same fashion for read 0 it is reduced by 75% and read 1 it is reduced by 46%. Finally SRAM with MTCMOS technique got better results than SRAM with DTCMOS technique.

VI. Conclusion

In this paper, reduction in leakage current which leads to reduction in delay and power dissipation as well as Power Delay product is analyzed for SRAM using DTCMOS and modified SRAM cell with MTCMOS technique using the Mentor Graphics Pyxis Schematic Editor 130-nm technology. It is found that total power consumption of proposed design with MTCMOS is reduced when compared to other SRAM cells. Hence the proposed SRAM cell with MTCMOS is Energy Efficient as its PDP value is less when compared to other conventional designs.

Acknowledgment

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