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Carrier Based Neutral Point Potential Regulator With Reduced Switching Losses For Diode Clamped Multilevel Inverter

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Abstract

Neutral Point Clamped converter, also called as three levelDiode Clamped Multilevel Inverter (DCMLI) offers several advantages such as lower voltage stresses, lower electromagnetic compatibility and better output. However, there is an important problem called Neutral Point Voltage (NPV) variation which leads to voltage unbalancing acrossa DC link andoutput waveform of the inverter.This variation happens due to the non-linearitiesin the circuit, non-linear loads, load unbalancing and nonuniform distribution of charges. In this paper, an NPV balancing strategy for Neutral Point Clamped (NPC) multilevel inverter isproposedand it is based on the Sinusoidal Pulse Width Modulation(SPWM). In this technique, an offset valuegetsadded to modulation wave to balance the NPVandits performanceis alsoanalyzed based on its THD and efficiency. It is also found thatthe reduction in switching losses is achieved when compared to conventional inverter.

Keywords: Diode Clamped Multilevel Inverter(DCMLI),Neutral Point Voltage (NPV), Neutral Point Potential (NPP), Offset Value.

Introduction

Multilevel converters are playing a vital role in high power application and demands. They can generate the output voltage and current of improved quality.There are several well knownmultilevel topologies as in [1].In this paper NPC inverter is discussed. Although NPC inverter has advantages over other topologies,the most important problem of NPC is balancing the DC link voltage [2] [3]. In [4] generation of control pulses for a Neutral Point Clamped inverterand its operationis discussed.To overcome unbalancing issue there are several control methods proposed earlier.The effects caused due to NPV imbalances and nonlinear loads are discussed.And the effects caused by negative sequence of output current, distortion due to both even and odd order harmonics are discussed in ref [5]. In [6] NPV is balanced and switching losses are reduced by insertion of zero switching zone with fundamental waves, but here we need load power factor angle which makes the control complex. Based on Hybrid Carrier based SVPWM on [7],NPV is balanced. A new neutral point balance strategy based on adding an offset voltage and factors such as NP current, NP voltage,power factor and regulation angle are given in[8].In [9] NPP is reduced by adding offset voltage with a half cycle of the fundamental wave.Earlier a control scheme with a state space model with feed forward algorithm is given, butimplementation of modeling is experimentally more complicated[10]. An analytical solution with zero sequence voltage is present, but its experimental implementation is critical[11].

In this research, toavoid the NPV unbalancing, an offset value gets added to modulation wave and NPV is balanced and its performance is compared with conventional inverter with unbalanced DC-link. In both cases, NPV their performances are analyzed based on their THD and efficiency as well as switching losses is also reduced when compared with conventional inverter.

Neutral Point Clamped Inverter

The circuit diagram of 3ϕ NPC inverter is pictured in Fig. 1. It is the combination of two 2-level VSI with some modification.

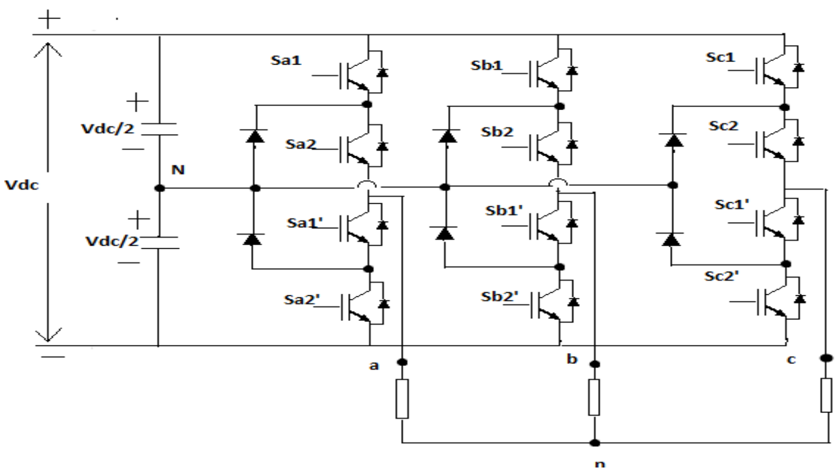

Figure 1: Circuit diagram of three phase 3L-NPC inverter

The common DC bus voltage gets shared by all the three phases of the inverter. The voltage shared by each capacitor is $\frac{Vdc}{(m-1)}$,here *m*is number of levels.

For *m*-level inverter, it has *m* phase voltage and *2* (*m-1*) line voltages. Diodes and switches involved in every phase are (*m*-1) * (*m*-2)and (*m*-1) respectively [4].

Operationof 3L-NPC Inverter

NPCinverter switching signals are *Sij*, where *I* represent the phases and *j* represents the switch numbering. Among the four switches only two switches receives the control signal. Other two receives the inverted signalto obviateshort-circuit in DC-link.

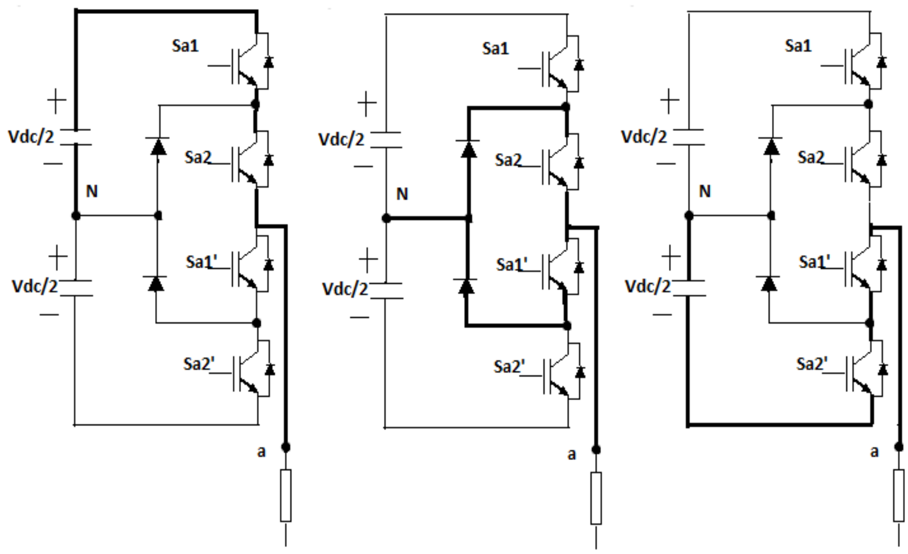

Figure 2: Switching operation of 3L-NPC inverter for phase “a”

The Fig. 2 shows the operation of 3L-NPC inverter,and also showsthat node “a” is connected to three level of the DC-link. And Table 1 shows the switching states.

Table 1
Switching states of 3L-NPC inverter for phase “a”

Voltage Level	**S1**	**S2**	**S3**	**S4**
Vdc/2	1	1	0	0
0	0	1	1	0
-Vdc/2	0	0	1	1

To make effective output, switching of the multilevel inverter is a very efficient one. There are several modulation techniques are available for multilevel inverter.

Block Diagram of NeutralPointpotential(NPP) Regulator

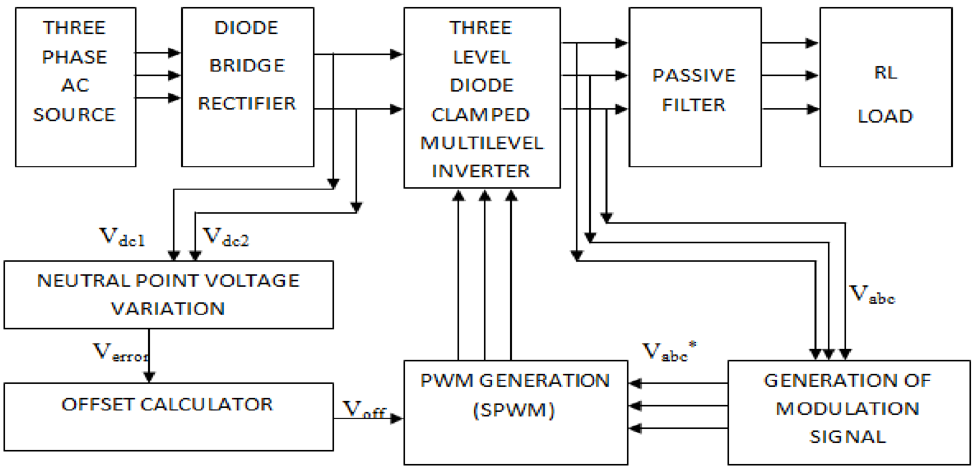

Figure3: Block diagram of NPP regulator based on SPWM technique

The block diagram for proposed scheme is shown in Fig.3.Here,incoming AC is convertedinto a suitable form for threelevel NPC inverter by the diode bridge rectifier. And the output of NPC inverter is fed to three phase RL load. In this method the switching for NPC inverter is given by using SPWM.

SPWM Technique

SPWM technique is the simplest modulation scheme as pictured in Fig. 4 where a sinusoidal waveform of desired frequency gets compared to high frequency carrier to get the pulses.Hoped pulses areaccomplished by changing the frequency and amplitude of the modulating wave.

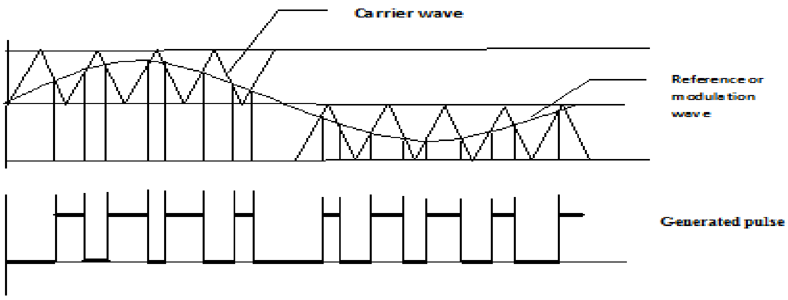

Figure 4: Pulse generation in SPWM technique

Design of Neutral Point Potential (NPP) Regulator

a. Generation of Modulation Signal Block:

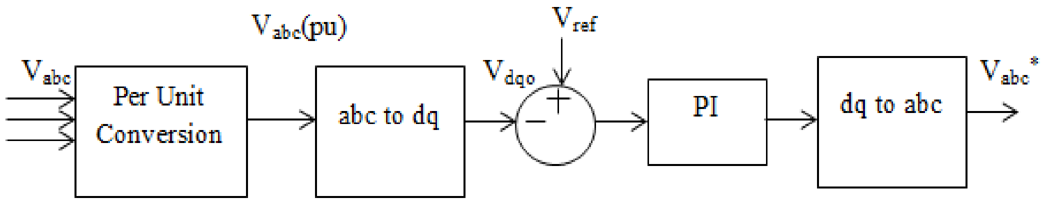

Figure 5: Proccess that takes place in Generation of Modulation Signal Block

As shown in Fig. 5, the inverter output voltage is converted into per unit and converted from abc to dq form for simplificationby following equation[9].

$$V_d = \frac{2}{3}[V_a \sin(wt) + V_b \sin(wt - 120^0) + V_c \sin(wt - 240^0)] \quad (1)$$

$$V_q = \frac{2}{3}[V_a \cos(wt) + V_b \cos(wt - 120^0) + V_c \cos(wt - 240^0)] \quad (2)$$

$$V_o = \frac{V_a + V_b + V_c}{3} \quad (3)$$

Then the error is processed through PI controller by taking k_p=0. 5 andk_i=10.And againdq form is convertedto abc form by following equation

$$V_a = V_d \sin(wt) + V_q \cos(wt) + V_o \quad (4)$$

$$V_b = V_d \sin(wt - 120^0) + V_q \cos(wt - 120^0) + V_o \quad (5)$$

$$V_c = V_d \sin(wt - 240^0) + V_q \cos(wt - 240^0) + V_o \quad (6)$$

b. Neutral Point Voltage Variation:

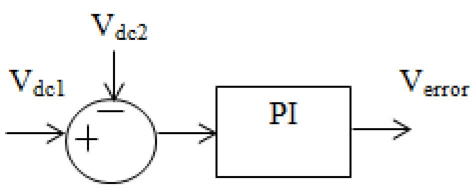

Figure 6: Calculation of Neutral Point Voltage Variation

Here the voltage variation in NP is analyzed by subtracting the voltageacross both the capacitor in DC bus as picture in Fig. 6.And the error is treated viathe PI controller.When the capacitor voltage difference is zero, then it means NPV is balanced. Then the output is fed to the offset calculator.

c. Offset Calculator:

In an offset calculator,the appropriate offset voltage for multilevel operation can be expressed as follows[7],so that comparisons between both reference and carrier wave generate optimized switching.

$$V_{off} = -\frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2} \quad (7)$$

$$V_{off}' = \frac{V_{dc}}{N-1} - \frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2} \quad (8)$$

d. PWM Generation:

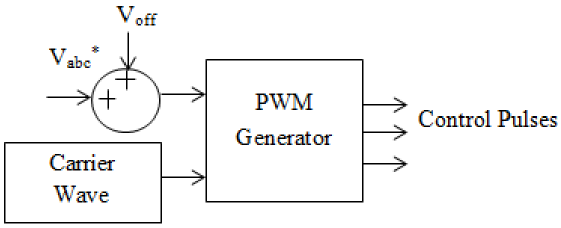

Figure 7: Pulse Generation for 3L-NPC Inverter

The abcoutput signalfrom the generation of modulation signal blockgets added to the offset value and given as a reference signal for modulation as pictured in Fig. 7.Then the reference signal is compared tothe triangular wave of high frequency whose output is given as the pulsefor the inverter.

Simulation Results

To show the effects of unbalanced DC link, the capacitor voltages are taken as different values.The output waveform in Fig.8 clearly shows that levels of the NPC inverter is not symmetrical and it is distorted.

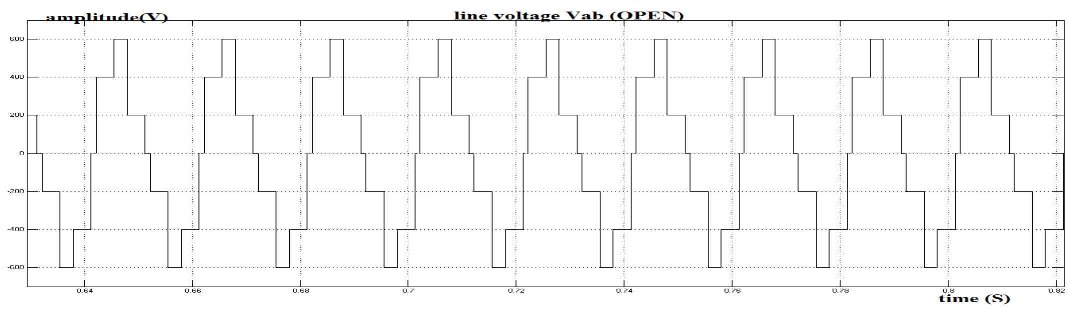

Figure8: Line voltage(V_{ab}) at the output side of inverter withunbalanced DC link withoutpassive filter

Theline voltage of inverter with passive filter is pictured in Fig.9. FFT analysis is donefor capacitor voltage Vdc1=200 and Vdc2=400 and the obtained THD is 9.01% as pictured in Fig.10.Due to unbalance in NPP, the harmonic content gets increased.

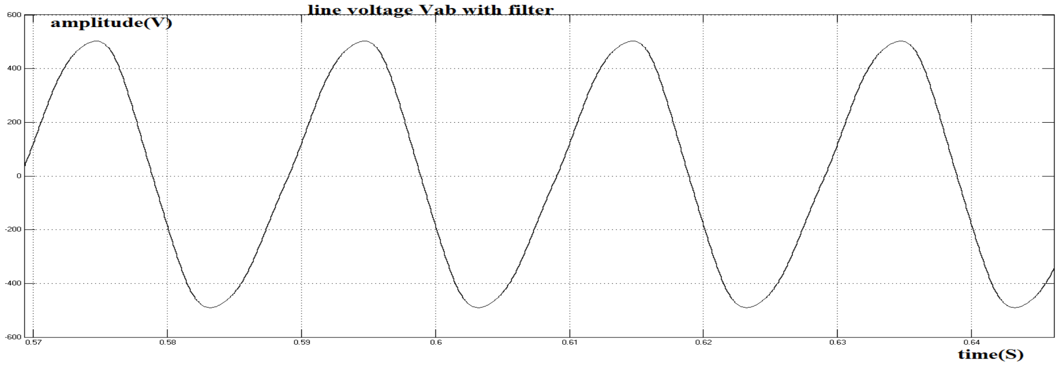

Figure9: Line voltage (V_{ab}) at the output side of inverter withunbalanced DC link with passive filter

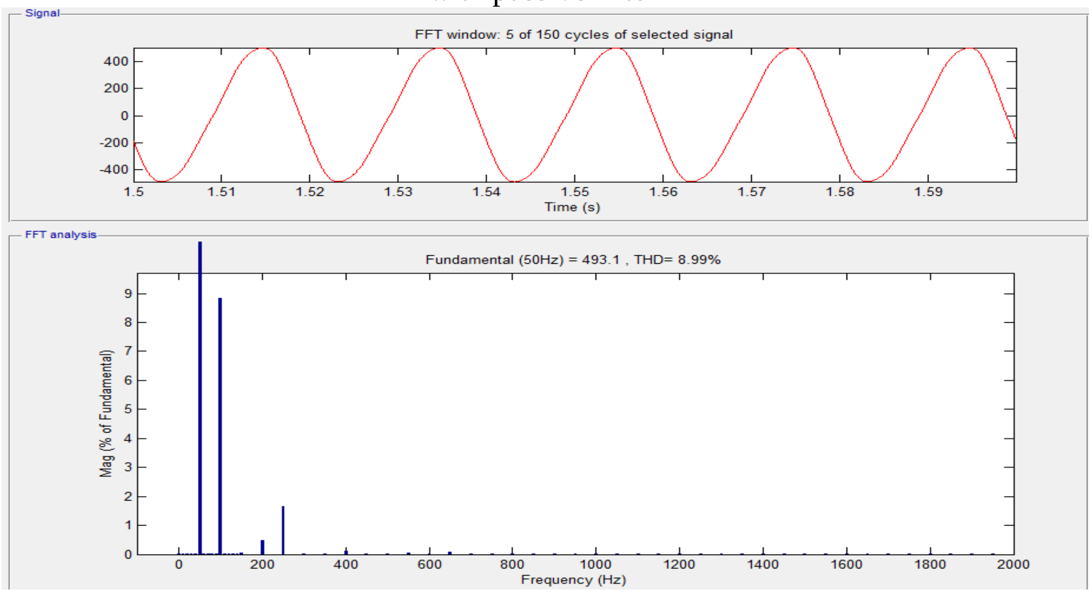

Figure10: THD obtained from line voltage (V_{ab}) at the output side of inverter underunbalanced DC link with passive filter

By using NPP Regulator, the NPV is balanced.Inverter output line voltage without and withpassive filterarepictured in Fig. 11 and Fig. 12.In which the distortions are reduced when compared to the unbalanced conventional inverter.

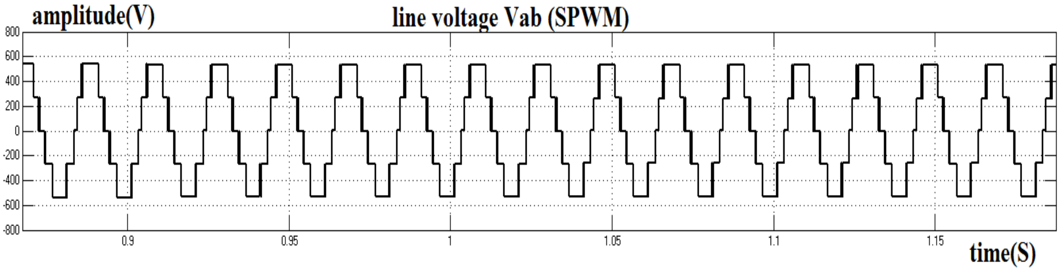

Figure 11: Line voltage (V_{ab})atthe output side ofinverterwith NPP regulator and without passive filter

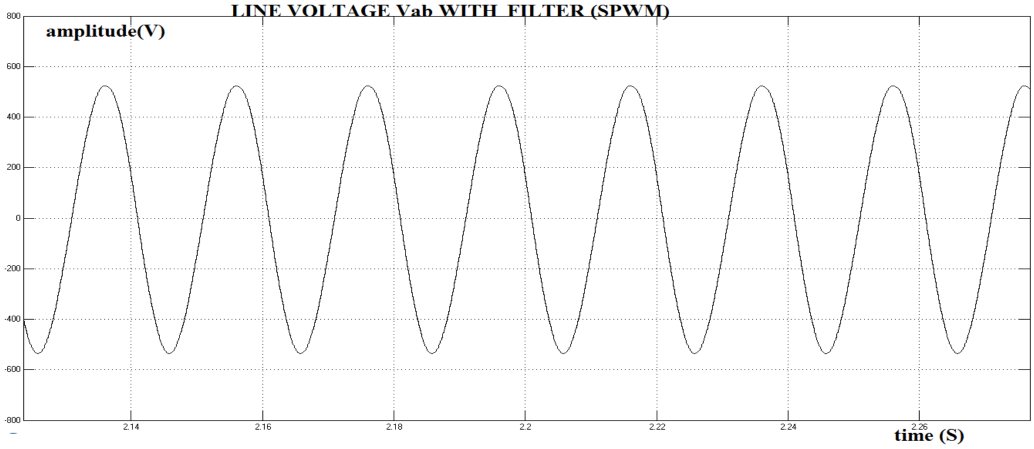

Figure 12: Line voltage (V_{ab})at the output side of inverterwith NPP regulator and passive filter

FFT analysis of inverter with filteris shown in Fig.13 in it the harmonic contents are reducedwhen compared to conventional inverter with unbalanced DC-link.

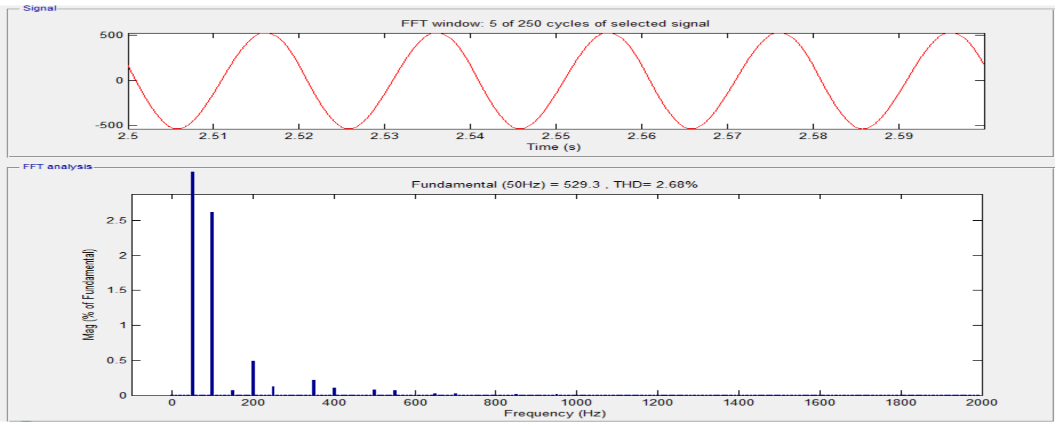

Figure 13: FFT analysis for output line voltage (V_{ab})ofinverter with NPP regulator and filter

The balanced NPP potential for three level DCMLI using NPP Regultor is pictured below in Fig. 14.

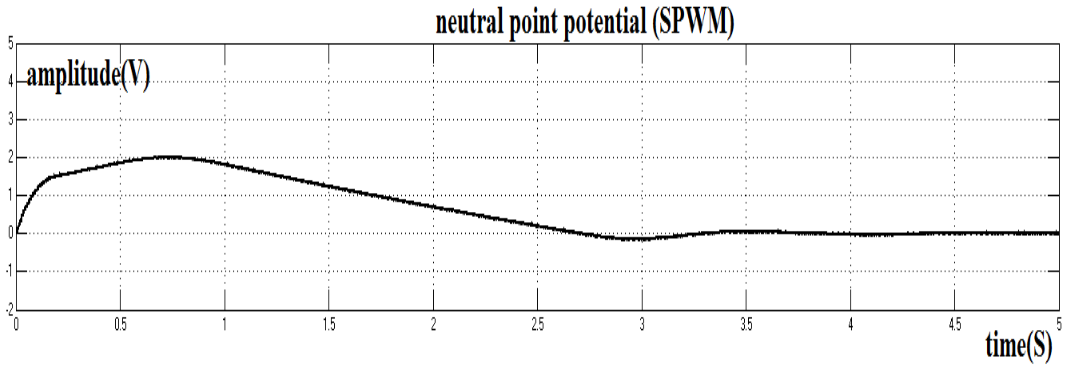

Figure 14: Balanced NPP using SPWM technique

The Table 2 shows the performance comparisons of conventional inverter and closed loop techniques with NPP Regulatorbased on their THD and efficiency. Where the efficiency of inverter increased by 2% than conventional inverter with unbalanced DC link.

Table2: Performance comparison based on THD and efficiency

Methods	**THD in %**	**Efficiencyin %**
CONVENTIONAL NPC INVERTER	9.00	86.54%
ADDING OFFSET VOLTAGE IN SPWM	2.68	88.76%

Switching Loss Calculation

To observe the diminution in switching losses,the efficiency of the inverter is measured. By using Efficiency Improvement Factor (EIF) reduced switching losses is verified[9].

$$EIF = \frac{\eta_1 - \eta_2}{\eta_2}$$

η_1 =efficiency of proposed inverter

η_2 =efficiency of conventional method

EIF obtained for SPWM is .02 Hence, improvement of about 2%in SPWM is observed.

Summaryand Conclusion

AnNPV balancing strategy for NPC converter based on SPWM is proposed. Here, the offset value gets added to the modulation wave to maintain the NPV balance. Switching losses are brought down when compared to conventional inverter.Besides maintaining the DC-link voltage, it also directs to diminution in the voltage distortion at the neutral point.Reduction in switching losses and improvement in performance of the proposed inverterareverified on the basis of Efficiency Improvement Factor (EIF).It indicates that the switching losses are considerably reduced and also there is an improvement in efficiency by using NPP Regulator when compared to conventional.

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