International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 7 (2015) pp. 18349-18360

http://www.ripublication.com

Congestion Adaptive Routing Techniques for 2D NOC

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Abstract

Network on Chip (NoC) is a new paradigm to make the interconnections inside a System on Chip (SoC).The main problem in network on chip is due to the congestion occur when transmitting the multiple data Packets. Congestion in network mainly occur due to multiple request at a same time. These congestion can be avoided by using path congestion aware adaptive algorithm for 3D NoC. In path congestion aware adaptive algorithm ,we can able to predict the traffic in both channel based information as well as switch based information ,whereas in previous techniques to determine the congestion only channel based information is used. Due to unavailability of switch based information, congestion in network is difficult to read. By using this path congestion aware adaptive algorithm we can able to find out possible congestion information and improve the selection of routing Path. Path congestion aware adaptive algorithm consist of two techniques: 1)path congestion aware selection strategy ,these techniques consider both the channel based as well as switch based information. 2) Contention Prediction techniques, these techniques determine the possible buffer size to determine the congestion.

Index: Network On Chip (NOC),Adaptive Routing, Congestion Techniques

1. Introduction:

According to Moore's Law, the complexity of each and every network is grows every each year. Much application needs low power, high performance systems, the number of computing resources in single chip is increased. In system on chip communication is achieved by means of bus interconnection. This bus interconnection needs arbitration logic to control the multiple bus request. Shared bus

interconnection has some limitation such as scalability, only one master at a time can utilize the bus. As number of bus used in the system increases, bandwidth require for interconnection is high when compared to current bus. These limitation can be overcome by using on chip packet. As the semiconductor technologies continuously grow each and every year, interconnection complexity of the network and congestion delay are the major drawbacks for the System on Chip.

To achieve and control congestion in network, network on chip should be scalable, flexible and reusable solution for the multiprocessor systems[1]. To gain the high throughput rate of the system, Network on Chip system should multiplexed the packet on channel and shares the data packets among the channel.

Due to congestion in packets result in unwanted and unpredictable delay for each packet flows in the network. When the size the network continuously grows, the traffic in the network becomes unbalanced in various applications [2]. By using load balancing mechanism aims to minimize the response time, resource reuse, maximize the throughput of the system.

Thus both channel and switch information results in unwanted delays in the routing path. By increasing the congestion delay network dissipates the large energy and dissipates the additional energy in the network.

Congestion in network can be avoided by using suitable algorithm. Adaptive algorithm is mainly used to reduce the congestion in the network. Adaptive algorithm ensures data packets from one node to another node even if more than one node is unavailable.

Congestion in the network consists of three types.

1. **Switch contention**: Each and Every packet compute for same output channel in the network (i.e., north) in the switch, contention occur.

2. **Switch Congestion**: when transmitting packet to particular output port some of the packet from input port received failed request from the output port is blocked and kept at the buffer. The routed packet should wait until the information is released.

3. **Channel Congestion**: Due to confined buffer size, the information in the switch is overflow. Due to confined buffer size, the information in the switch is overflow. Due to overflow of data congestion occur in the channel.

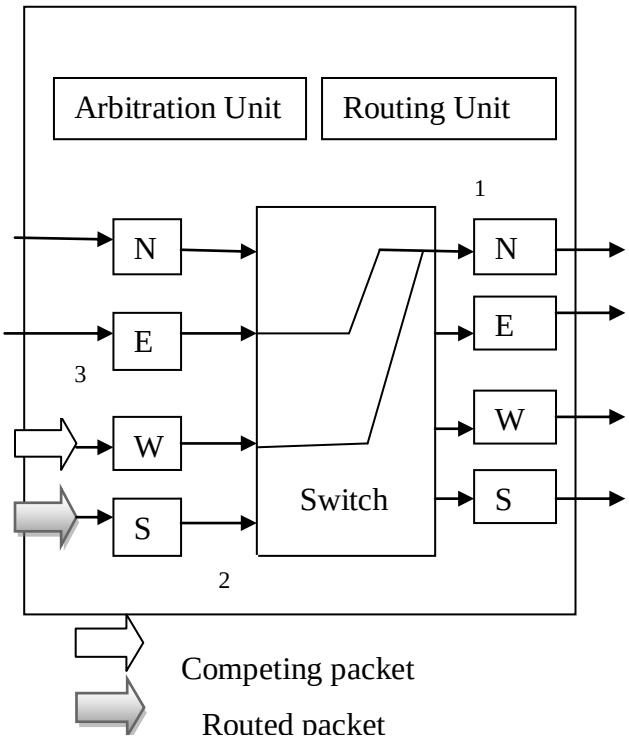


Fig 1. Types of congestion

Thus in network both channel and switch based congestion are correlated, switch congestion occur one router and simultaneously channel congestion will occur in other router. Thus congestion in each and every router continuously grows and the performance of the system is highly affected.

Adaptive algorithm determines path for each data packets flows. This data packets flows is determined by predefined rule. The routing algorithm consists of routing function as well as selection function. The routing function produces a group of output channels based on the deadlock free turns model[3] and selection function produce only one output channels at a time [4]. The performances of the system are affected by selection function. To detect the path congestion in the network we should consider both routing unction and selection function.

In conventional techniques only channel base information is used to detect the congestion status. In path congestion aware adaptive routing algorithm is proposed to determine latency for each packets passing in the router. This algorithm considers both the channel as well as switch congestion.

2. Proposed Routing Techniques:

Routing is the process of transmitting data packets from sources to destination**.** The ultimate goals of routings are correctness, simplicity and fairness.

Routing algorithms are classified as adaptive routing algorithm and non adaptive routing algorithm. Adaptive routing algorithm changes their routing decisions to change in traffic and in topology. These algorithm adjacent the router when one or two nodes are unavailable. Non–adaptive routing algorithm does not change their routing decision.

Path Congestion Aware Adaptive Algorithm

To achieve high throughput, NOC multiplexes the data on channel and shares the data throughout the network. Packet contention problem in switch results in unpredictable delays for each data flow. Contention problem in switch result in unwanted delays. As the size of the devices increases result in increased delay in the routing.

Path Congestion Aware Adaptive Routing algorithm works as follows:

1. Path Congestion Aware Selection Strategy: this method required fine grained congestion information of adjacent routers. This strategy considers both channel as well as switch congestion.

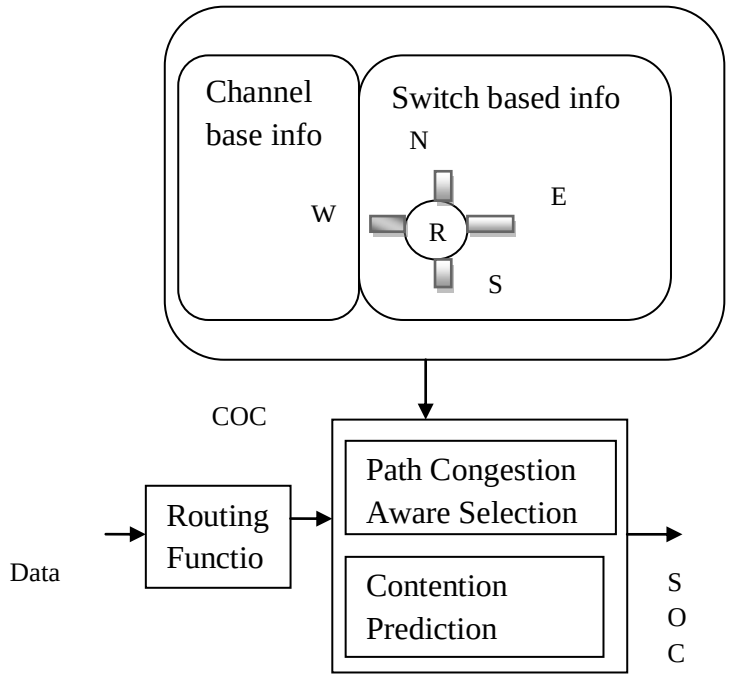
2. Contention Prediction Techniques: Due to the insufficient buffer size, congestion occurs in the channel. By increasing buffer level, determine the congestion for the system performances.

The advantage of Path congestion aware routing is deadlock free routing model.

Path Congestion aware routing algorithm consist of path congestion aware selection function. This function works under two techniques as follows

1. Path Congestion Aware Selection strategy: This strategy is based on both channel congestion and switch congestion information.

2. Congestion Prediction Techniques: This techniques changes capacity of buffer level to route the next information to determine whether congestion is occurred in adjacent path.



COC: Candidate output channel

SOC: Selected output channel

Fig 2 Path Congestion Aware Adaptive Algorithm

3.Block diagram of Path Congestion Aware Adaptive Routing Algorithm

A data stream is a sequence of digitally encoded signal is used to transmit the data to the row buffer. A row buffer is a data buffer used in the modern DRAM chips that allow quick and easy access to the multiple data located in the physical row in the memory.

A memory bank consists of multiple rows and columns of storage units and usually occupied in many chips. In a single read or write operation, only one bank is accessed. The size of a bank is determined by bits in a column and a row, per chip× number of chips in a bank. Memory bank operation is controlled by finite state machine.

A finite-state machine (FSM) model of computation used to design for sequential logic circuits. The data obtained from data stream is stored in buffer in First In First Out manner.

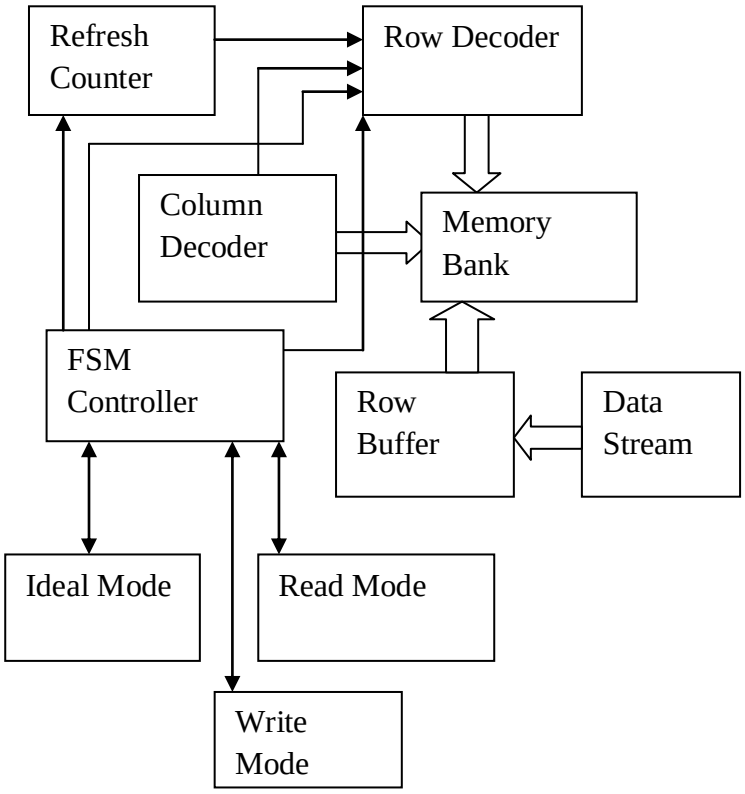


Fig 3 Block Diagram of PCAR Router

FSM controller perform three operations namely write, idle mode, read mode. To perform next operation refresh counter is used

FSM is used to controls the read and write operation of FIFO. When FIFO is empty then FSM controller performs write operation. When FIFO is full then FSM controller performs read operation. Otherwise the FSM controller is in ideal mode.

In this method no load bypass is used between memory and processor to increase the throughput. So, no need to store the incoming bits in memory. When memory is empty input bits will be bypasses into next stage and reduce the latency. Priority based routing approach will efficiently increased the throughput. By means of state transition method this techniques avoid use of buffers.

4. Experimental Results

Path Congestion Aware Adaptive Routing is simulated using Modelsim 6.4 and synthesis using quartus II tools. The simulation results is shown in Fig4

If priority p1 is set, then information travel from North to west and assign the value 96 in north port. If congestion occur then, assign value to east port as 96 otherwise assign value to south port as 456.

If priority p2 is set, then information travel from North to east and assign the value 1396 in north port. If congestion occur then, assign value to west port as 96 otherwise assign value to south port as 1396

If priority p3 is set, then information travel from North to south and assign the value 1396 in north port. If congestion occur then, assign value to west port as 96 otherwise assign value to east port as 1396.

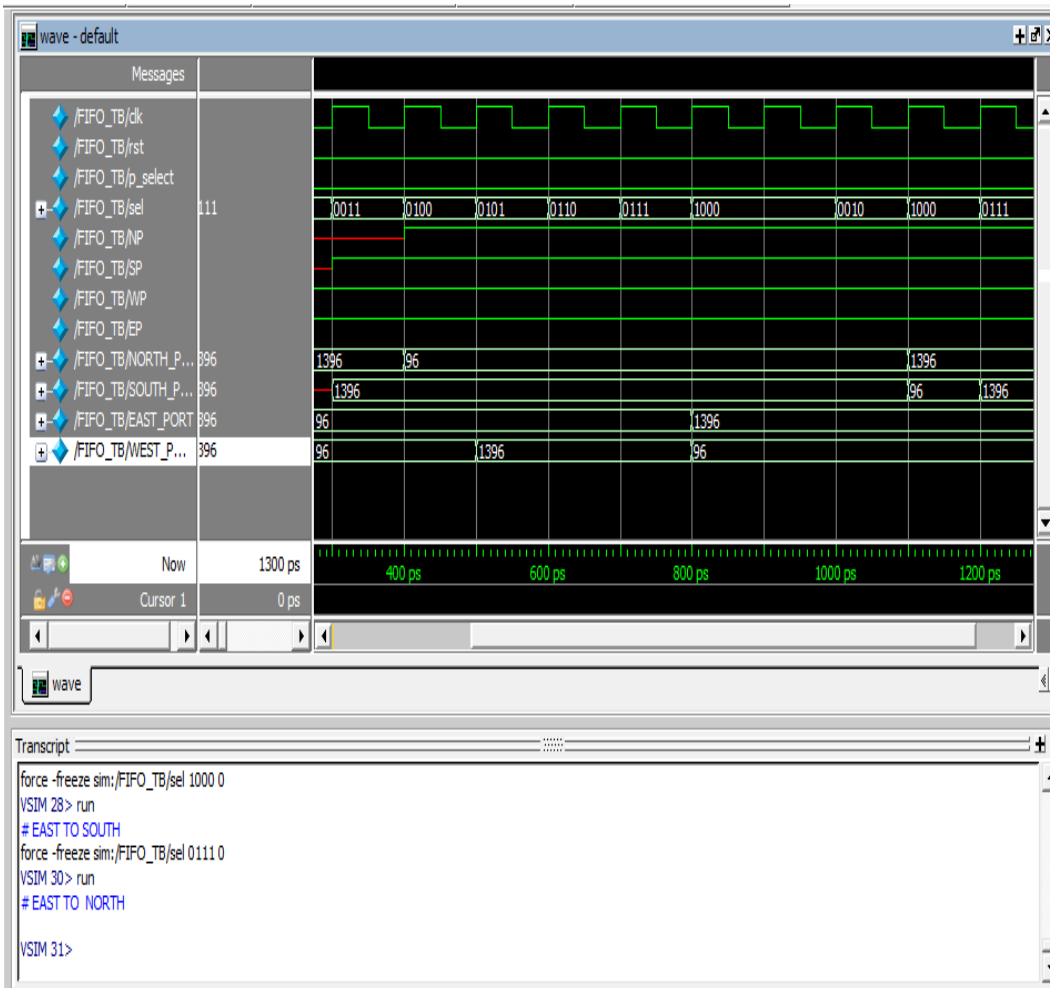


Fig 4. Simulation Results of Routing Algorithm

If priority p4 is set, then information travel from west to North and assign the value 1396 in north port. If congestion occur then, assign value to south port as 96 otherwise assign value to east port as 96.

If priority p5 is set, then information travel from West to east and assign the value 1396 in west port. If congestion occur then, assign value to south port as 96 otherwise assign value to east port as 96.

If priority p6 is set, then information travel from west to South and assign the value 1396 in west port. If congestion occur then, assign value to east port as 96 otherwise assign value to north port as 96.

If priority p7 is set, then information travel from east to west and assign the value 96 in east port. If congestion occur then, assign value to south port as 96 otherwise assign value to west port as 96.

If priority p8 is set, then information travel from east to north and assign the value 1396 in east port. If congestion occur then, assign value to south port as 96 otherwise assign value to north port as 96.

Otherwise the information travel from east to north and assign the value 1396 in east port. If congestion occur then, assign value to south port as 96 otherwise assign value to north port as 96.

The synthesis report of area, power, time is shown in following figure .The synthesis report of area for Path Congestion Adaptive Routing is shown in Fig 5

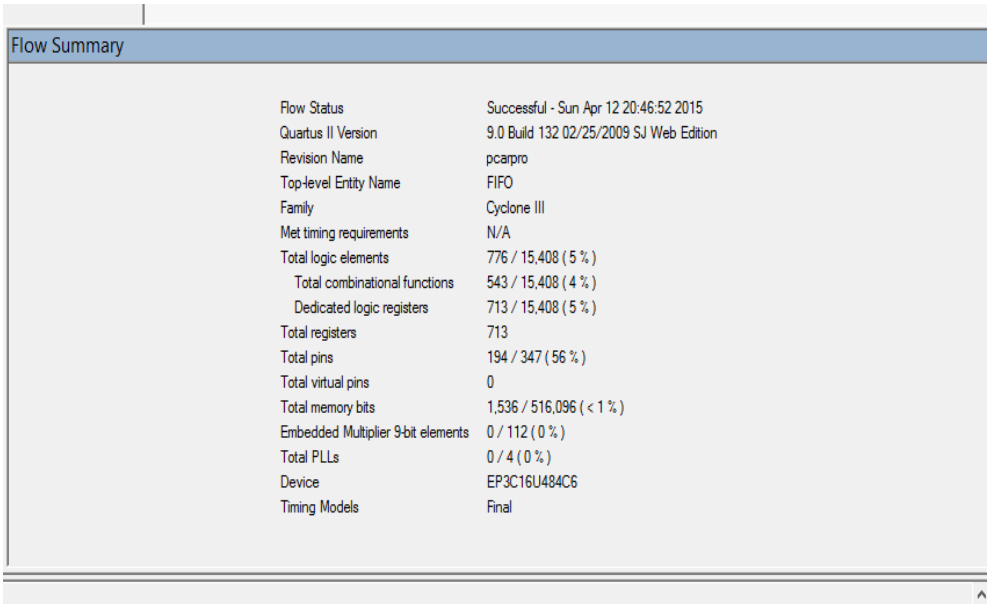
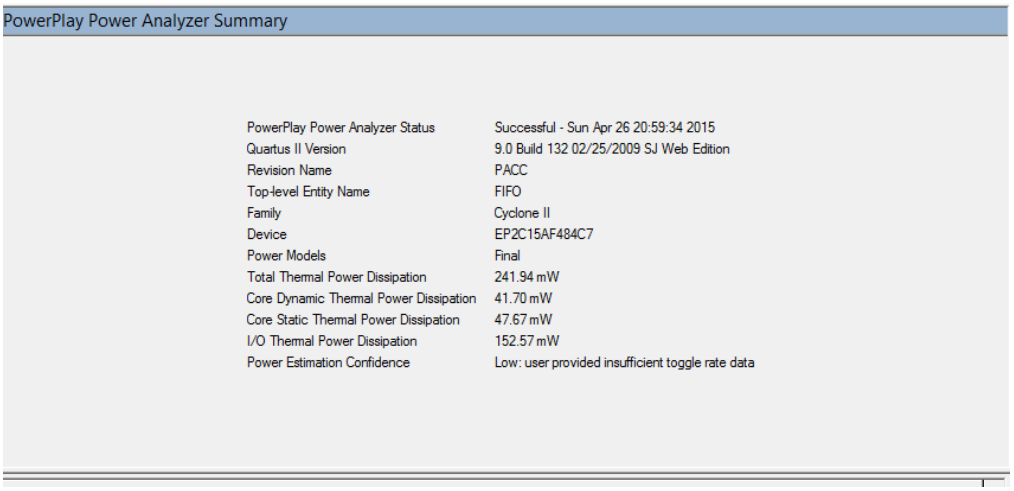


Fig 5 Synthesis Report of Area for Path Congestion Adaptive Routing

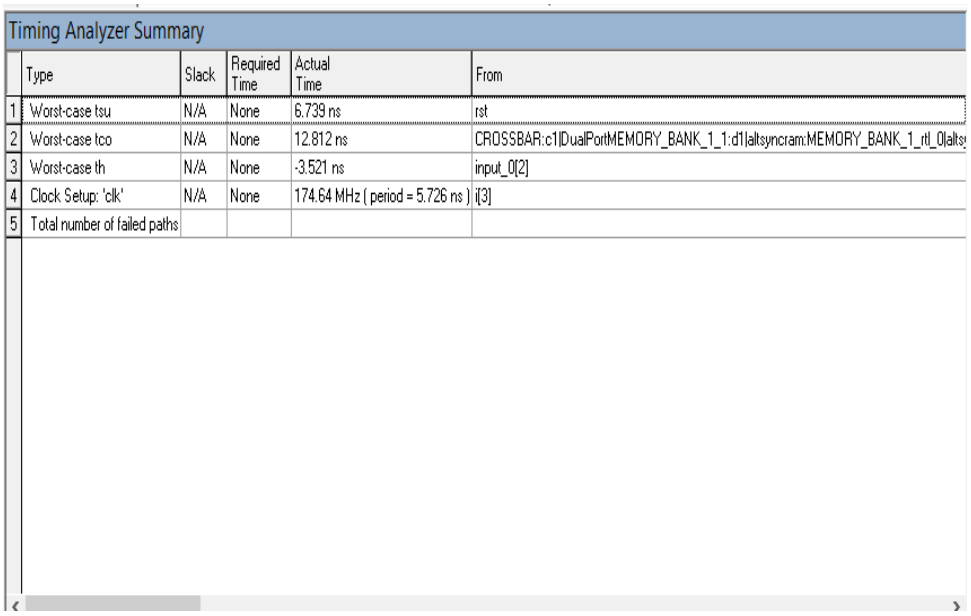
The synthesis report of Power for Path Congestion Adaptive Routing is shown in Fig 6


PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Sun Apr 26 20:59:34 2015
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	PACC
Top-level Entity Name	FIFO
Family	Cyclone II
Device	EP2C15AF484C7
Power Models	Final
Total Thermal Power Dissipation	241.94 mW
Core Dynamic Thermal Power Dissipation	41.70 mW
Core Static Thermal Power Dissipation	47.67 mW
I/O Thermal Power Dissipation	152.57 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig 6 Synthesis Report of Power for Path Congestion Adaptive Routing

The synthesis report of Time for Path Congestion Adaptive Routing is shown in Fig 7


Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From
1	Worst-case tsu	N/A	None	6.739 ns	rst
2	Worst-case tco	N/A	None	12.812 ns	CROSSBAR:c1|DualPortMEMORY_BANK_1_1:d1|altsyncram:MEMORY_BANK_1_rtl_0|alts
3	Worst-case th	N/A	None	-3.521 ns	input_0[2]
4	Clock Setup: 'clk'	N/A	None	174.64 MHz (period = 5.726 ns)	i[3]
5	Total number of failed paths				

Fig 7 Synthesis Report of Time for Path Congestion Adaptive Routing

The synthesis results are tabulated as follows

Parameter	Percentage
Area	776/33,216(2%)
Total Thermal Power Dissipation	241.94mw
Timing Analysis	6.729 ns

5. Conclusion

The Path Congestion Aware Routing algorithm considers both switch congestion and channel congestion. By this algorithm Path Congestion Aware Selection strategy and Contention Prediction Technique is designed. Path Congestion aware selection Strategy reduced the path congestion information on the adjacent routers. Congestion Prediction Techniques changes the buffer level to predict the possible congestion. Thus overall area occupied is 2% and total power Consumption used in this routing is about 241.94 mw

6.References

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Biographies

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