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New Inverter Topology for Independent Control of Multiple Loads

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Abstract

The compact and cost-effective fifteen switch inverter for multiphase output is proposed in this paper for hybrid energy vehicle. The proposed topology of fifteen-switch three leg inverter is capable of generating twelve phase output voltage (four groups of three phases) from the single common dc bus. This topology reduces the switch count from twenty four as in conventional method to control four three phase loads to fifteen. In this paper, comparison of SPWM and ZSVPWM switching techniques used for this inverter topology are presented. The analysis of voltage and current THD and fundamental values is done with different switching techniques.

Keywords: fifteen switch inverter, zero space vector PWM, spwm, zero sequence signal component

INTRODUCTION

Inverters are has been widely used as dc/ac converters to control voltage and frequency of ac loads. Recent development in application like electric vehicles (EV) and hybrid electric vehicles (HEV) has offered many challenges to the power electronics industry. There are many applications where two or more ac loads require independent control. The application such as traction system, hybrid vehicle, helicopters, robotics etc deals with more than one motor. In particular, there are two methods of controlling four motors i.e providing two separate nine switch inverters [1-7] to drive four motor or connecting the four motors in parallel and driving them with a single inverter. While designing power electronics circuitry is to reduce the number of active and passive element.

To operate a standard motor at rated power and rated speed a pulse width modulated inverter cannot supply sufficient voltage with pure sinusoidal modulation. To overcome this issue in recent past Space Vector Pulse Width Modulation (SVPWM) switching technique is developed and widely used for three phase PWM inverter and the multilevel inverter [8]-[9]. Space vector modulation strategies offer better performance as compared to regular pulse width modulation. The advantages offered by space vector modulation technique is in terms of reduced harmonic current ripple, optimized switching sequence and increased voltage transfer ratios. The voltage can be generally increased by harmonic suppression for the rectifiers as well as inverters. This can be mainly done by injecting the third harmonic component with fundamental in balanced three phase loads [10]-[11].

This paper presents the analysis and comparison of the Zero Space Vector PWM (ZSVPWM) with respect to the conventional SPWM technique of the fifteen switch inverter topology. The need of control scheme in view of four independent motor operations is achieved with independent operation of variable speed drives applications. The inverter operation and its performance are evaluated using MATLAB/SIMULINK for simulation of this inverter topology.

STRUCTURE OF FIFTEEN SWITCH INVERTER

Basic Structure

The proposed structure of Fifteen Switch inverter is shown in Figure 1, which consists of Four Three phase inverters combined with nine common switches. The four, three phase inverters are named as Inv1, Inv2, Inv3 and Inv4. The Inv1 consists of switches SR1, SR2, SY1, SY2, SB1, SB2, Inv2 consists of switches SR2, SR3, SY2, SY3, SB2, SB3, Inv3 consists of switches SR3, SR4, SY3, SY4, SB3, SB4 and Inv4 consists of switches SR4, SR5, SY4, SY5, SB4 and SB5.

The gating signal is generated by pulse width modulator (PWM) for Inv1, Inv2, Inv3 and Inv4 as shown in Fig. 3. This PWM modulator has single carrier waveform and four reference waveform. The reference waveform for Inv1 and Inv2 are with positive dc shift and are above zero level of carrier signal. The reference waveform for Inv3 and Inv4 are with negative dc shift and are below zero level of carrier signal.

REALIZATION BY PWM METHOD

The conventional triangular carrier based PWM method is adopted for all four inverters. The four sinusoidal reference signals are required for controlling the output voltages of this inverter. The pulse width modulation of *Inv₁ and Inv₂* is obtained at the upper part of a carrier wave, and the pulse width modulation of *Inv₃ and Inv₄* is obtained at its lower part, as shown in Figure 2.

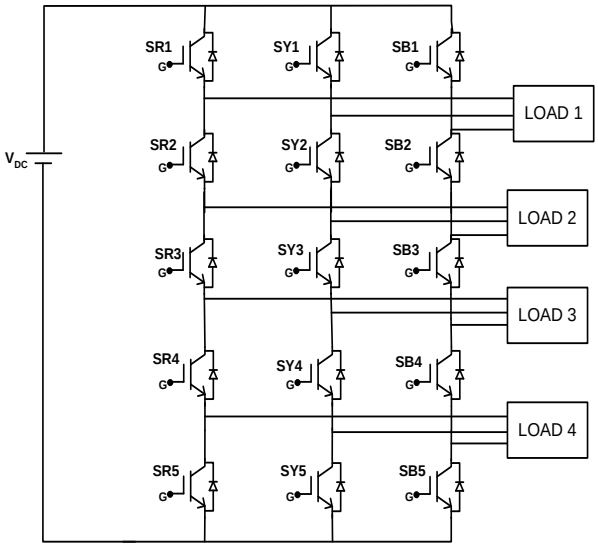


Figure 1: Main circuit of proposed fifteen-switch inverter

Let voltage reference of R phase for *Inv1, Inv2, Inv3 and Inv4* are V_{R1}^{ref}, V_{R2}^{ref}, V_{R3}^{ref} and V_{R4}^{ref} respectively. Assume that V_{R1}^{ref}, V_{R2}^{ref}, V_{R3}^{ref} and V_{R4}^{ref} are given by

$$V_{R1}^{ref} = A_1 \sin(2\pi f_1 t + \emptyset_1) + offset1 \quad (1)$$

$$V_{R2}^{ref} = A_2 \sin(2\pi f_2 t + \emptyset_2) + offset2 \quad (2)$$

$$V_{R3}^{ref} = A_3 \sin(2\pi f_3 t + \emptyset_3) + offset3 \quad (3)$$

$$V_{R4}^{ref} = A_4 \sin(2\pi f_4 t + \emptyset_4) + offset4 \quad (4)$$

Where A_1, A_2, A_3 and A_4 are amplitudes, f_1, f_2, f_3 and f_4 are frequencies, and ϕ_1, ϕ_2, ϕ_3 and ϕ_4 are phases for V_{R1}^{ref}, V_{R2}^{ref}, V_{R3}^{ref} and V_{R4}^{ref} respectively. A general modulation rate m is given by

$$m = \frac{V^{ref}}{V_{dc}/2} \quad (5)$$

Where V_{dc} is a dc source voltage. An offset of $3V_{dc}/8$ and $V_{dc}/8$ is added to the reference in (1) and (2) respectively. Similarly an offset of $-V_{dc}/8$ and $-3V_{dc}/8$ is added to the reference in (3) and (4) respectively when calculating the proposed PWM modulation. Therefore

$$m_1 = \frac{V_{R1}^{ref} + 3V_{dc}/8}{V_{dc}/2} = \frac{V_{R1}^{ref}}{V_{dc}/2} + \frac{3}{4} \quad (6)$$

$$m_2 = \frac{V_{R2}^{ref} + V_{dc}/8}{V_{dc}/2} = \frac{V_{R2}^{ref}}{V_{dc}/2} + \frac{1}{4} \quad (7)$$

$$m_3 = \frac{V_{R3}^{ref} - 3V_{dc}/8}{V_{dc}/2} = \frac{V_{R3}^{ref}}{V_{dc}/2} - \frac{3}{4} \quad (8)$$

$$m_4 = \frac{V_{R4}^{ref} - V_{dc}/8}{V_{dc}/2} = \frac{V_{R4}^{ref}}{V_{dc}/2} - \frac{1}{4} \quad (9)$$

The range of the reference is $-Vdc/8 \le V_{Rx}^{ref} \le Vdc/8$ where x =1, 2, 3 and 4 for Inv1, Inv2, Inv3 and Inv4 respectively. The method for generation of gate pulses is shown in Fig.4.

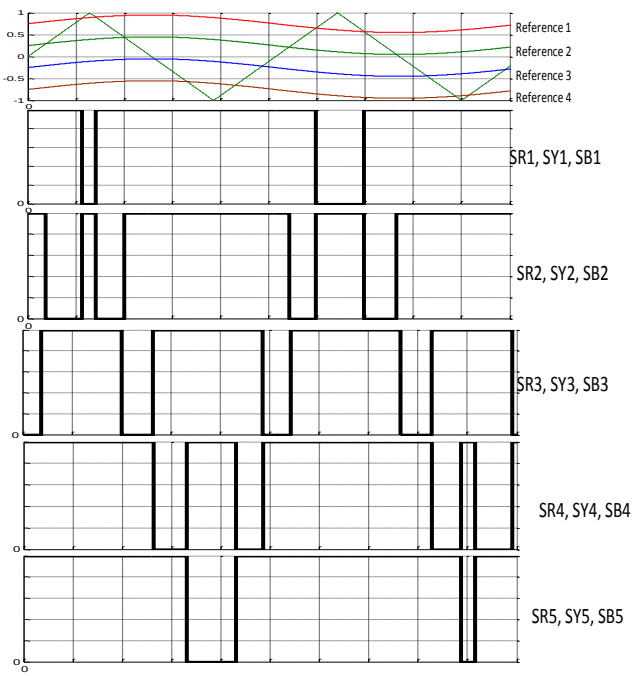


Figure 2: Principle of operation

The block diagram for generation of pulses for all the five switches in a phase is shown in Fig.4.

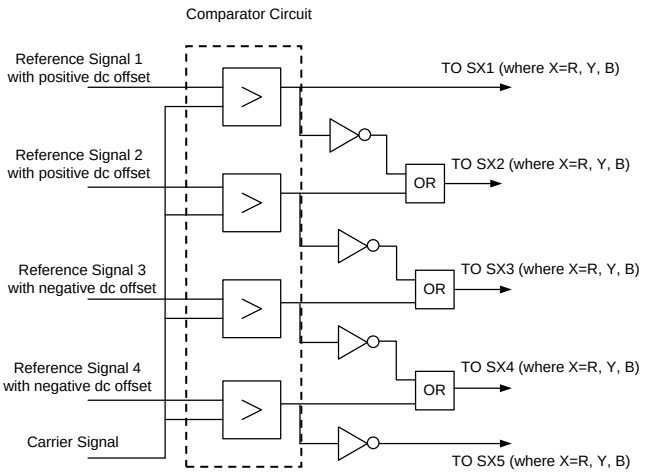


Figure 3: Bock diagram representation for pulse generation

Design Of ZSVPWM

To put on some benefits in the performance of the inverter appropriate triplen is added. The desired waveform is given by

$$y = \sin\omega t + A\sin 3\omega t \qquad (10)$$

Optimum distortion calculation

To generate the Phase voltage with zero third harmonics can be generated by adding third harmonics in the reference sinusoidal waveform. This method improves the efficiency of class B inverters by producing the flat tapped phase waveforms. The desired waveform of the type

$$y = \sin\omega t + A\sin 3\omega t$$

To get the optimal value of Y the variable A is to be determined. It can be obtained as

$$\frac{dy}{dt} = \cos\omega t + 3A\cos 3\omega t = 0$$

The maxima & minima of the waveform therefore occur at

$$\cos\omega t = 0 \quad \textit{and} \quad \cos\omega t = \left(\frac{9A-1}{12A}\right)^{\frac{1}{2}}$$

$$\sin\omega t = 1 \quad \textit{and} \quad \sin\omega t = \left(\frac{1+3A}{12A}\right)^{\frac{1}{2}}$$

Using identity, we get

$$y = (1+3A)\sin\theta - 4A\sin^3\theta$$

Substituting the values of sinθ obtained, we get

$$\hat{y} = 1 - A \quad \textit{and} \quad \hat{y} = 8A\left(\frac{1+3A}{12A}\right)^{\frac{3}{2}} \qquad (11)$$

The optimum value of A is that value which minimizes $\hat{y}$ and can be found by differentiating the expression for $\hat{y}$ and equating it to zero. Thus the values of A are

$$A = \frac{-1}{3} \quad \textit{and} \quad A = \frac{1}{6}$$

The value of $\hat{y}$ cannot be greater than unity for this reason we discard the value A= -1/3. The required value of A is therefore 1/6, and the required waveform is

$$y = \sin\theta + \frac{1}{6}\sin 3\theta \qquad (12)$$

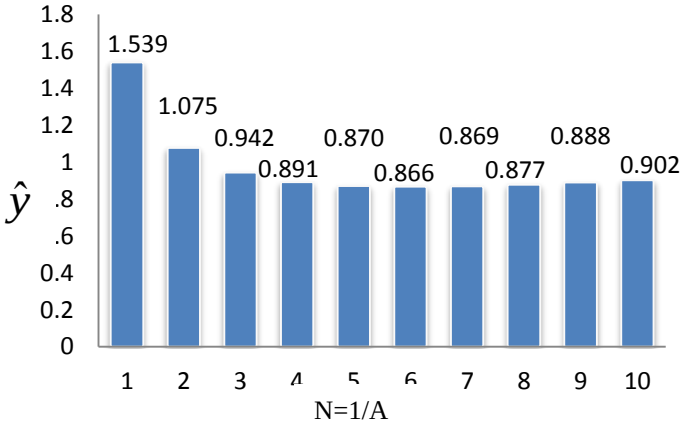


Figure. 4. Grahical representation of (11), $\hat{y}$ is minimum at A=1/6

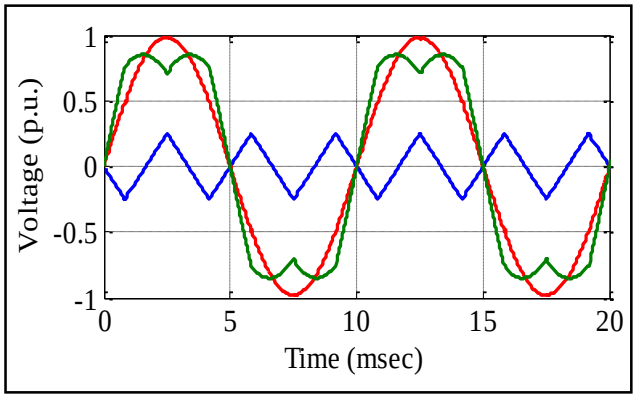


Figure. 5. Waveform of fundamental signal (Red), Third harmonic signal (Blue) and resultant signal (Green)

Performance of inverter

The nine switch inverter is simulated and its control signals are derived in MATLAB/SIMULINK.

Table I: Inverter parameters

DC Bus Voltage	100 V
Carrier frequency	2 kHz
Load	30 Ω & 100mH
Reference Frequency	50Hz

Zero sequence component generator

The zero sequence voltage generator is made up with three phase Diode Bridge and an inverting adder. At the output of the bridge voltages are given by V_A and V_B, along with the output voltage of the inverting adder is shown in the Figure 6. The generated zero sequence waveform is used further in SVPWM operation.

Generation of Switching Signals

The block diagram for generation of the switching pulses in SPWM and ZSVPWM mode is shown in the Figure 7. The Switch 'S' is used toggle between SPWM and SVPWM technique. When the switch is open the inverter operates with SPWM technique and with switch closed it works with ZSVPWM technique. The upper reference & lower reference is added with zero sequence signal as shown in Figure 7 having frequency three times of fundamental frequency. The resultant is then passed through comparator which compares the modified signal with the carrier signal of frequency 2 KHz.

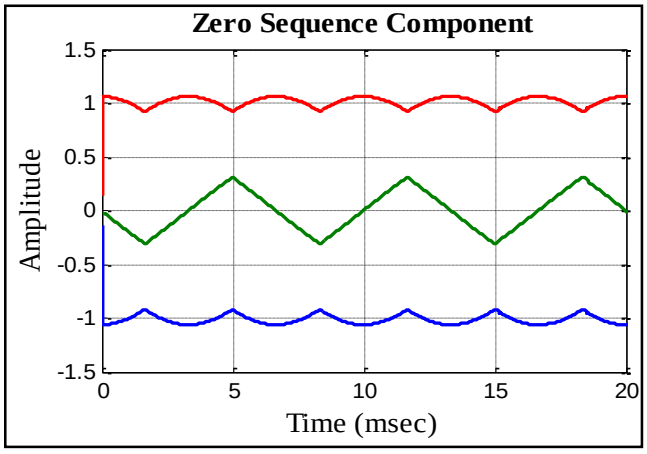


Figure 6: Zero sequence component

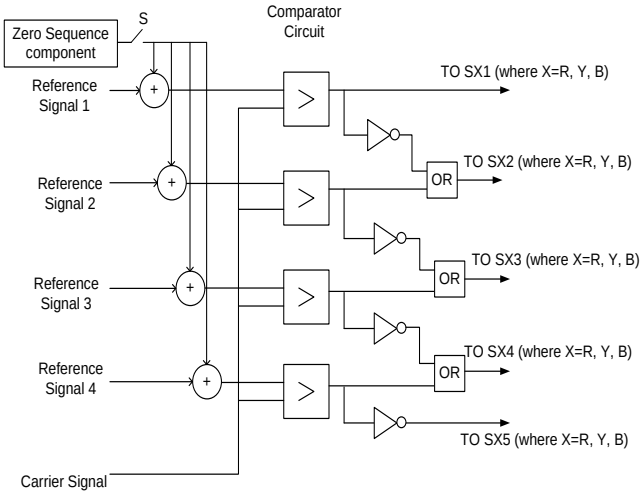


Figure 7: Generation of Gating Pulse for SPWM & ZSVPWM technique

Analysis of Voltage and Current

The line voltage and phase voltage of four ac loads for SPWM are shown in Figure 8 & Figure 9 respectively. The phase shift in reference signal 2, reference signal 3 & reference signal 4 is 30 degree, 60 degree and 90 degree with respect to reference signal 1. It can be clearly observed that the output voltage frequency is same as reference frequency for four loads, which conclude that all the loads can operate independently. The line currents in four loads are shown in Figure 10.

The analysis of voltage and current is done using MATLAB/ simulink with SPWM and SVPWM with equal four loads. The values of THD and fundamental rms values for line voltage, phase voltage and current are given in Table III. It can be clearly observed that there is 1.15 times increment in the fundamental rms value of voltage and current with SVPWM technique compared to SPWM technique. The graphical representation of THD and fundamental values of voltage and current is shown in Figure 11 & Figure 12.

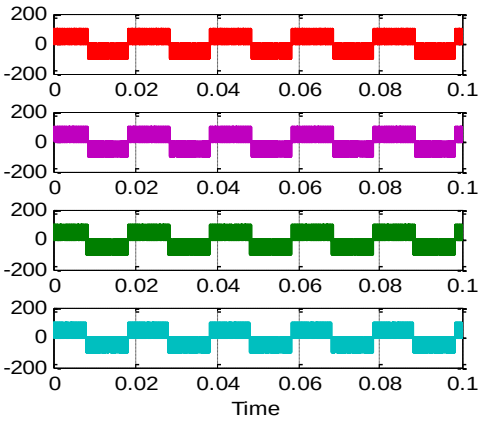


Figure 8: Line voltage of four RL load at frequency of 50Hz with different phase shift with SPWM technique

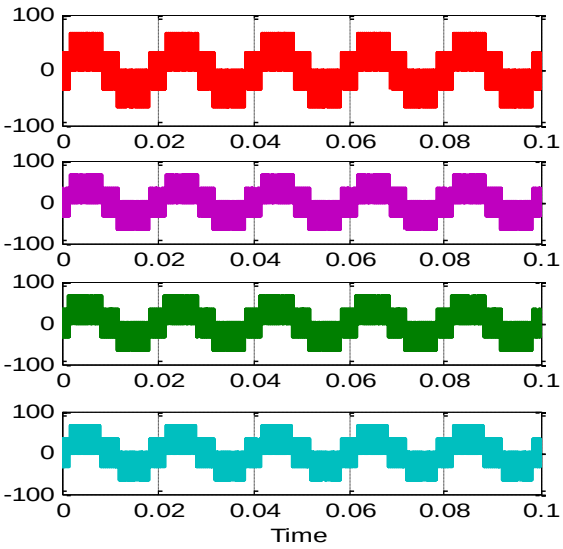


Figure 9: Phase voltage of four RL load at frequency of 50Hz with different phase shift with SPWM technique

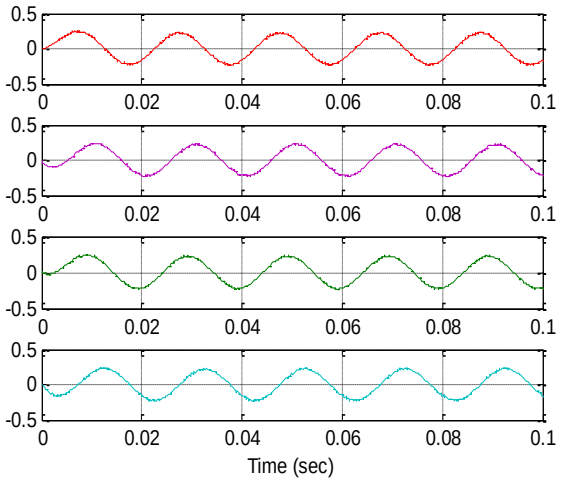
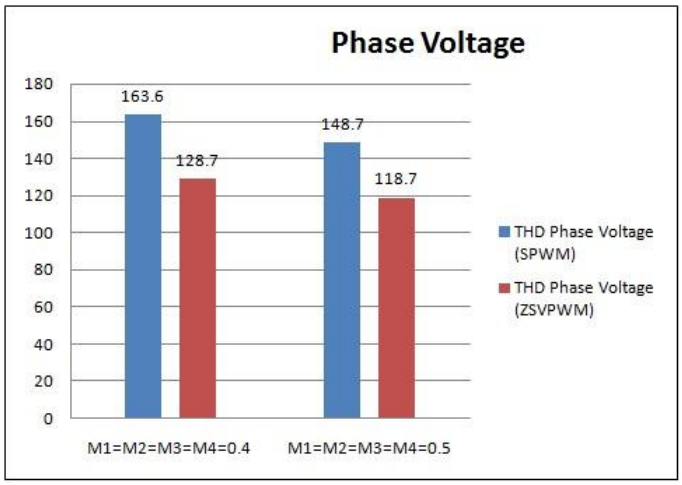
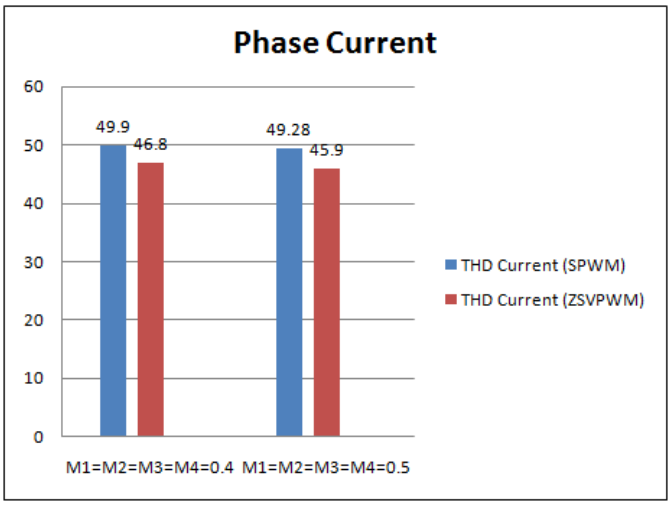


Figure 10: Load Current of four RL load at frequency of 50Hz with different phase shift with SPWM technique

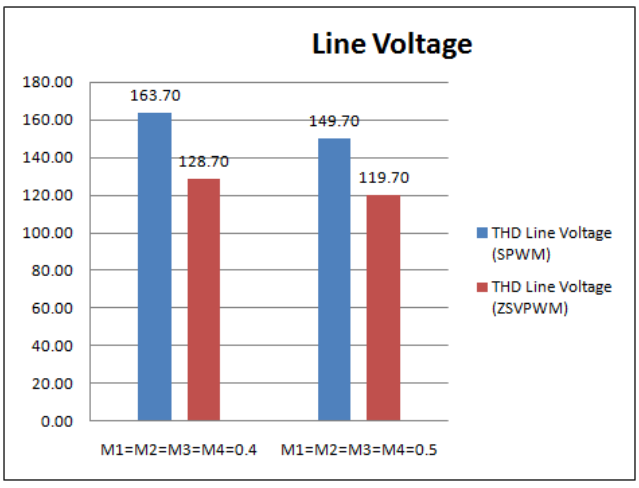


(b)

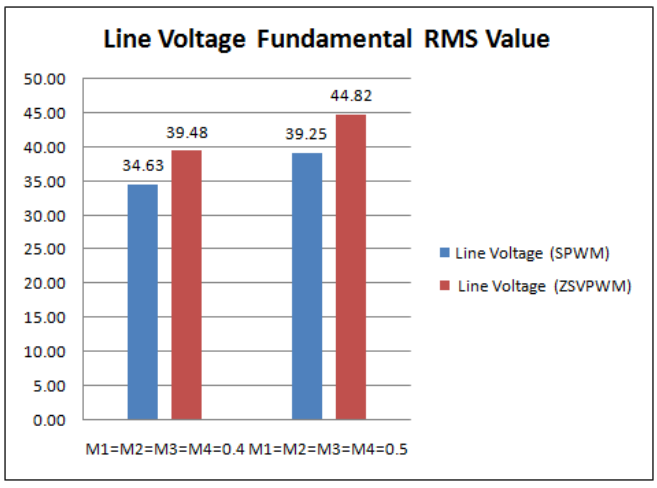


(c)

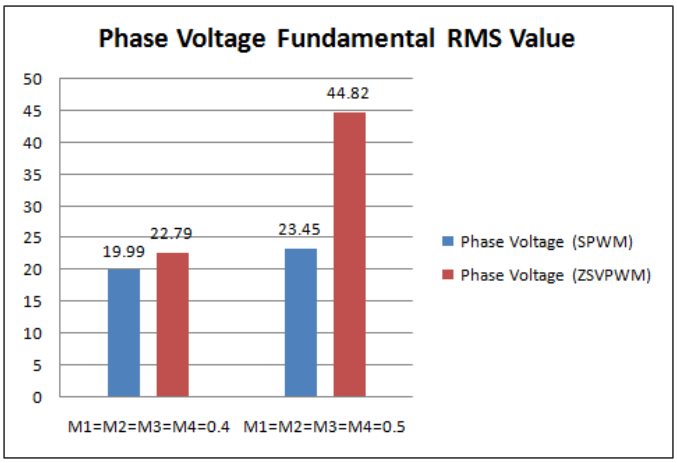
Figure 11: Comparison of THD of Load-1 of R phase with SPWM and ZSVPWM technique of (a) Line Voltage (b) Phase Voltage (c) Phase Current



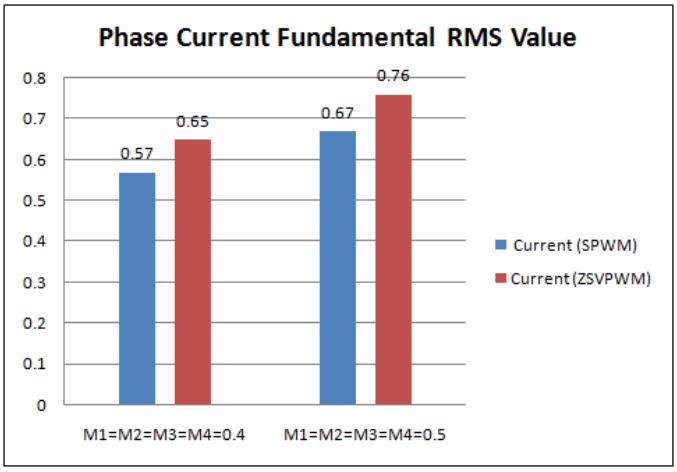
(a)



(a)



(b)



(c)

Figure 12: Comparison of Fundamental RMS of Load-1 of R phase with SPWM and ZSVPWM technique of (a) Line Voltage (b) Phase Voltage (c) Phase Current

Hardware Implementation

The prototype of fifteen switch inverter is built. The load connected is resistive load of same rating. The pulses for fifteen switch inverter are generated using Digital Signal Controller (DSC) dsPIC33EP512MU810. The pulses from DSC are then passed through the buffer circuit. Then this pulse is given to isolation circuit and driver circuit. The power circuit consists of the MOSFET IRF 840 (8A, 500V) as switching device. dsPIC33EP512MU810 is a new kind of DSC chip of Microchip. It is a 100 pin IC with 512kbram. The actual hardware setup is shown in Figure 13. The pulses generated after the buffer circuit is shown in Figure 14. It can be observed that at any instant of time only four pulses is in high state.

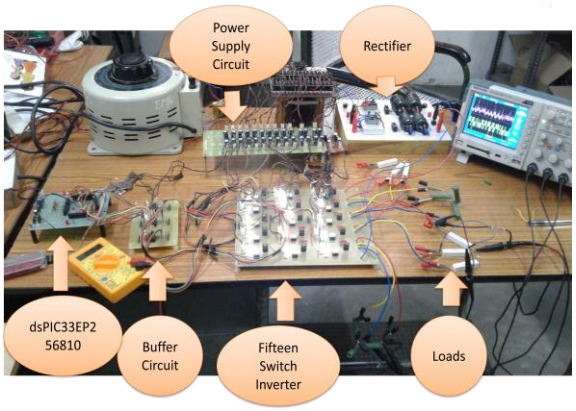


Figure 13: Hardware setup

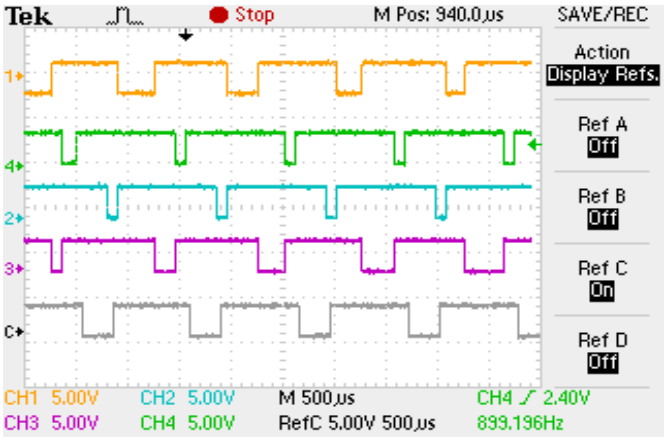


Figure 14: Generated pulses for switch SR1, SR2, SR3, SR4 and SR5

The line and phase voltage of Load 1, Load 2, Load 3 and Load 4 with dc link voltage of 20V and SPWM technique is shown in Figure 15 and Figure 16 respectively. The connected load is of value R=30ohms and L=100mH

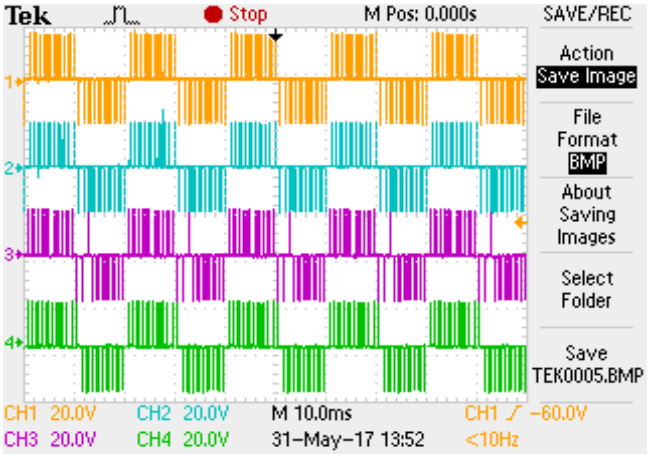


Figure 15: Line voltage of Load 1, Load 2, Load 3 and Load 4 respectively DC link voltage = 20V with SPWM technique

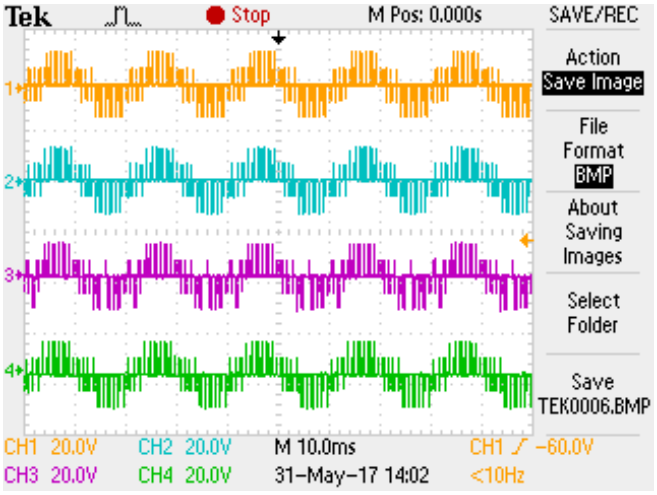


Figure 16: Phase Voltage of Load 1, Load 2, Load 3 and Load 4 respectively DC link voltage = 20V with SPWM technique

CONCLUSION

The operation of proposed topology of fifteen switch inverter with SPWM and SVPWM is simulated and their performance has been presented. The independent control is feasible with each of the three phase load. It is possible to operate these loads from the same DC bus having better DC bus utilization. The effectiveness of ZSVPWM technique in this operation improves the inverter output rms voltage for a given DC bus voltages as compare to SPWM. The inherent advantages of the fifteen switch inverter are its cost effectiveness and improved reliability due to less switch count.

Table III

Values Total Harmonic Distortion and Fundamental RMS of Line Voltage, Phase Voltage & Current at different Modulation index for SPWM and ZSVPWM technique for Load-1 R phase (carriers frequency= 2 kHz)

Modulation Index		SPWM						ZSVPWM					
		Line Voltage		Phase Voltage		Current		Line Voltage		Phase Voltage		Current	
	THD (%)	Fundamental RMS (V)	THD (%)	Fundamental RMS (V)	THD (%)	Fundamental RMS (A)	THD (%)	Fundamental RMS (V)	THD (%)	Fundamental RMS (V)	THD (%)	Fundamental RMS (A)	THD (%)
M1=M2=M3=M4=0.4		**163.70**	**34.63**	**163.60**	**19.99**	**49.90**	**0.57**	**128.70**	**39.48**	**128.70**	**22.79**	**46.80**	**0.65**
M1=M2=M3=M4=0.5		**149.70**	**39.25**	**148.70**	**23.45**	**49.28**	**0.67**	**119.70**	**44.82**	**118.70**	**26.78**	**45.90**	**0.76**

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