

A Low Power MCML Non-Sequential Phase Detector

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Abstract

By the using of MCML circuits, a 4 GB/s clock non-sequential phase detector circuit is designed in a 0.35 μ m CMOS technology. The power dissipation of proposed phase detector is much smaller than the conventional complementary pass transistor logic (CPL) phase detector. The implemented MCML phase detector consumes 0.7688nW when operating upto 4GHz clock frequency with 3.3V supply voltage. The conventional CPL phase detector consumes 4.7856nW when operating upto 2GHz clock frequency. The modified phase detector can be used in high speed and low power consumption applications.

Index terms: MCML, Phase locked loop, power consumption, VCO.

Introduction

Phase locked loop are important in several of applications such as frequency synthesis, clock recovery and wireless communication system [1]. It is used as clock or carrier generator. These applications need low power operation and long battery life. Phase detector is one of the main blocks of PLL. The function of phase detector is to detect the phase change in input signal. A phase detector can monitor the difference between input data and clock. It generates an UP signal if the input data leads the clock and a down signal if input data lags the clock [2]. The output node voltage of the charge pump is charged or discharged controlled by UP and DOWN [3].

This paper proposed a design of 4GHz CMOS MCML phase detector circuit. The conventional phase detector was implemented by using CPL scheme which can operate upto 2GHz of clock frequency. The use of MCML is quite impressive due to its phenomineous applications like high speed and low power consumption. The simplest MCML structure is the buffer which consists of a differential pair and

resistive loads. The operational principle of MCML is similar to that of the differential amplifier [4].

The paper is organized as follows: Architecture of phase detector with complementary pass transistor (CPL) is explained in section II. In section III, the new phase detector circuit with MCML is introduced and its functionality is explained. Section IV shows the simulation results and conclusion is drawn in section V.

Architecture of Phase Detector

The architecture of non-sequential phase detector based on even number of VCO stage is shown in figure 1.

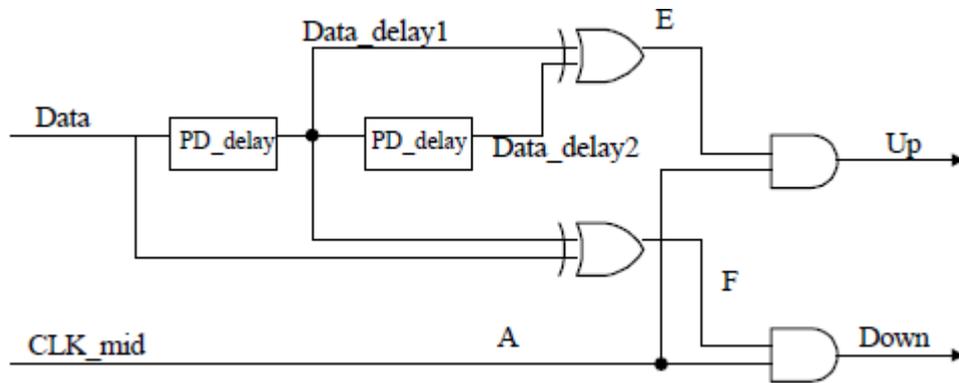


Figure 1: Phase Detector based on VCO even number of stages.

Here, the architecture of phase detector shows the use of two XOR gates, two delay cells and two AND gates [5]. Delay cells are used to provide delay in input data at two stages as shown in figure 1. After applying delay1, XOR operation is providing between the data and delay 1 which produces an output signal named as F. Similarly, XOR operation of delay1 and delay2 produces an E signal. These E and F signals are responsible for producing UP and DOWN signals. The UP and DOWN signals that are required to drive the charge pump are generated from signals A, E and F [5].

Delay Cell

Two delay cells have been used in the phase detector [5]. Simply, delay is provided by using a number of inverters connected in series. Delay time requirement can be easily varied and controlled by using this configuration of delay. Figure 2 shows the delay cell using six inverters.

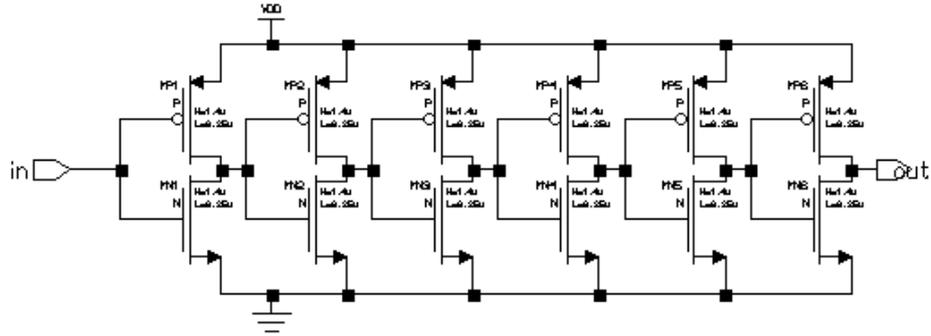


Figure 2: Delay Cell

CPL gates

To implement CPL XOR and AND gate six transistor have been used in each gate out of which four are NMOS transistors and two PMOS transistors [5]. Complementary signals are present at the both input and output of each logic gates. The use of complementary pass transistor logic gives the reduction in the parasitic capacitance. Figure 3(a) & (b) shows the CPL XOR and CPL AND gates.

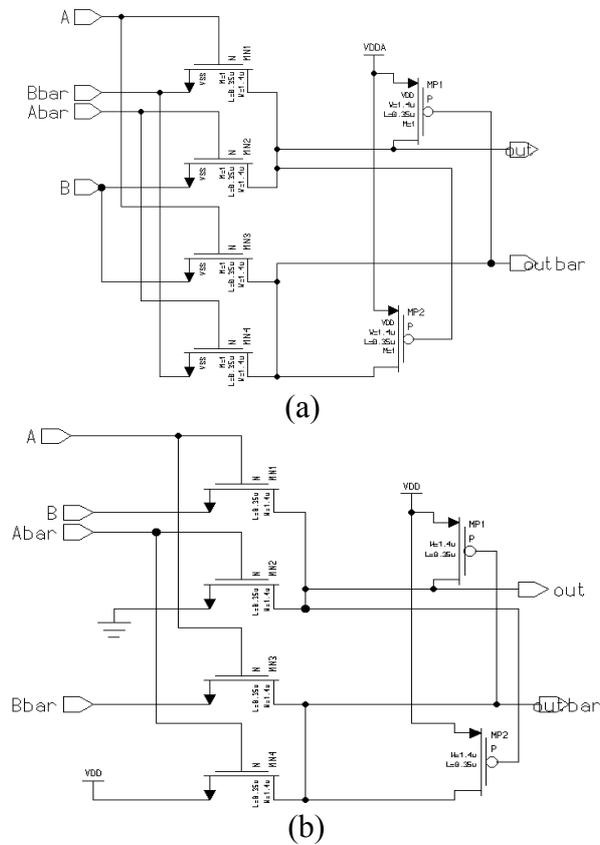


Figure 3: (a) CPL XOR (b) CPL AND gates

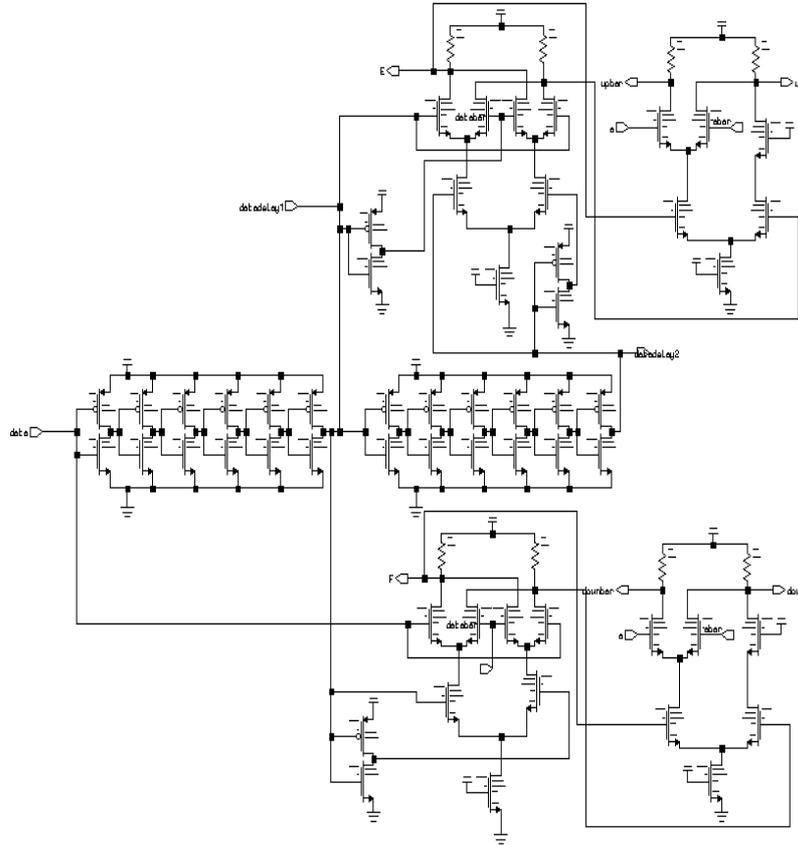


Figure 7: MCML phase detector.

Simulation Results

Table 1 summarizes the power consumption and maximum frequency of two phase detector. Results of power consumption are obtained with reference frequency of 45MHz. Phase detector with CPL gates shows power consumption of 4.7856nW and detect the signal of maximum frequency upto 2GHz. Phase detector with MCML gates shows power consumption of 0.7688nW and detect the signal of maximum frequency upto 4GHz.

Table 1: Phase detector's performance summary.

PHASE DETECTOR	CPL_PD[5]	MCML_PD (Present work)
Power Consumption (nW)	4.7856	0.7688
Maximum frequency (GHz)	2.0	4.0

Phase detector using conventional complementary pass transistor logic (CPL) and modified MOS current mode logic (MCML) has been successfully simulated and

studied in $0.35\mu\text{m}$ standard digital CMOS technology. The simulated output waveforms of CPL and MCML phase detector are shown in figure 8. After simulating, it is observed that the maximum operating frequency of CPL phase detector is 2 GHz and modified MCML phase detector is 4 GHz. Operating voltage $V_{DD} = 3.3\text{V}$ is taken for each phase detector.

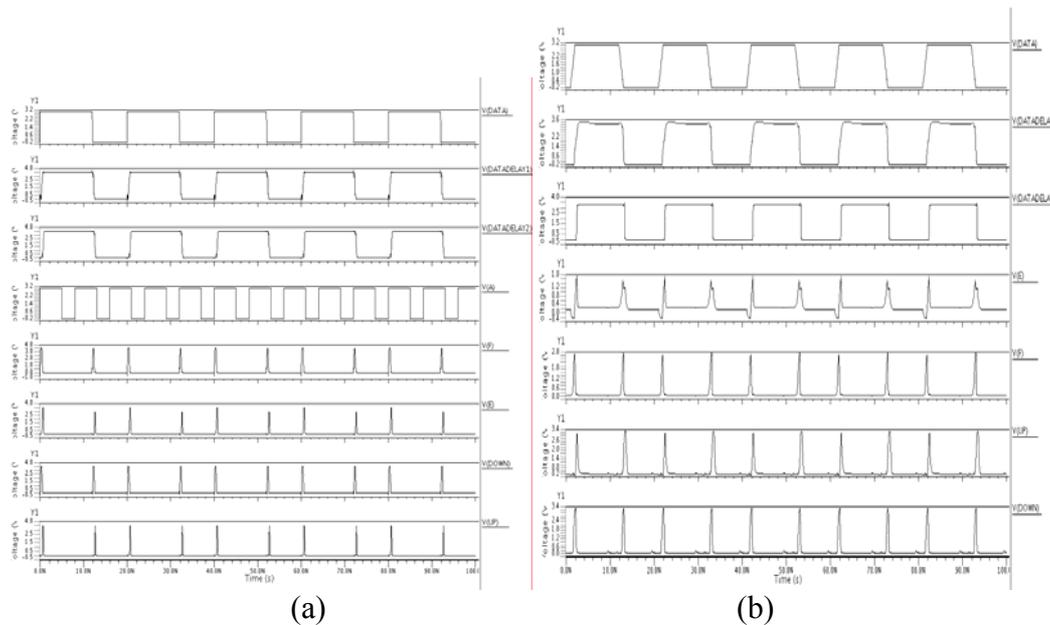


Figure 8: Output waveforms of phase detectors. (a) PD_CPL OUTPUT (b) PD_MCML OUTPUT

Conclusion

This paper gave an overview of several important design considerations for low power and high speed CMOS phase detector circuits design. These designs include the use of simple structure using MCML gates. A non-sequential MCML phase detector has been designed where power consumption of phase detector is 0.7688nW and maximum operating frequency is 4 GHz.

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